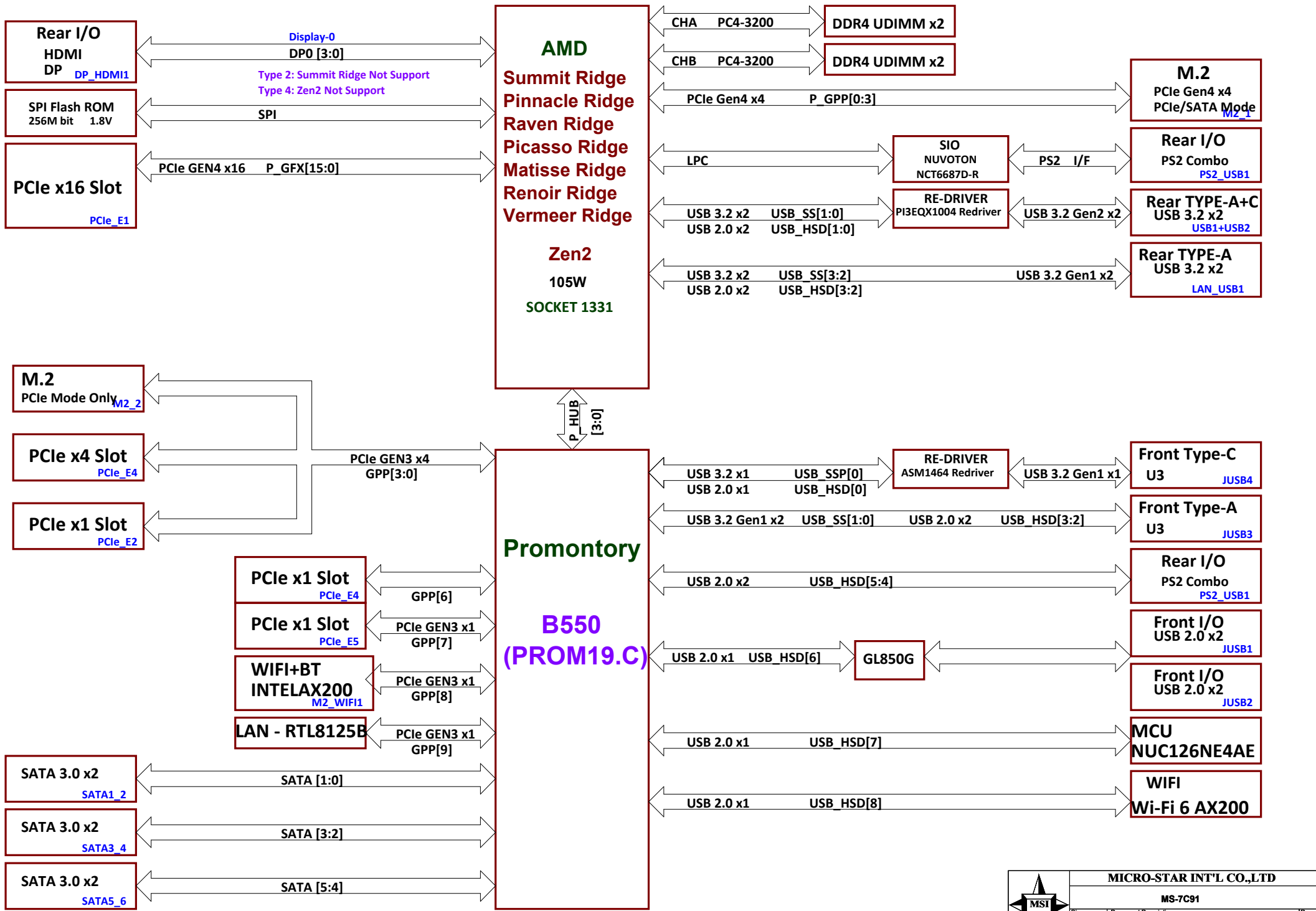
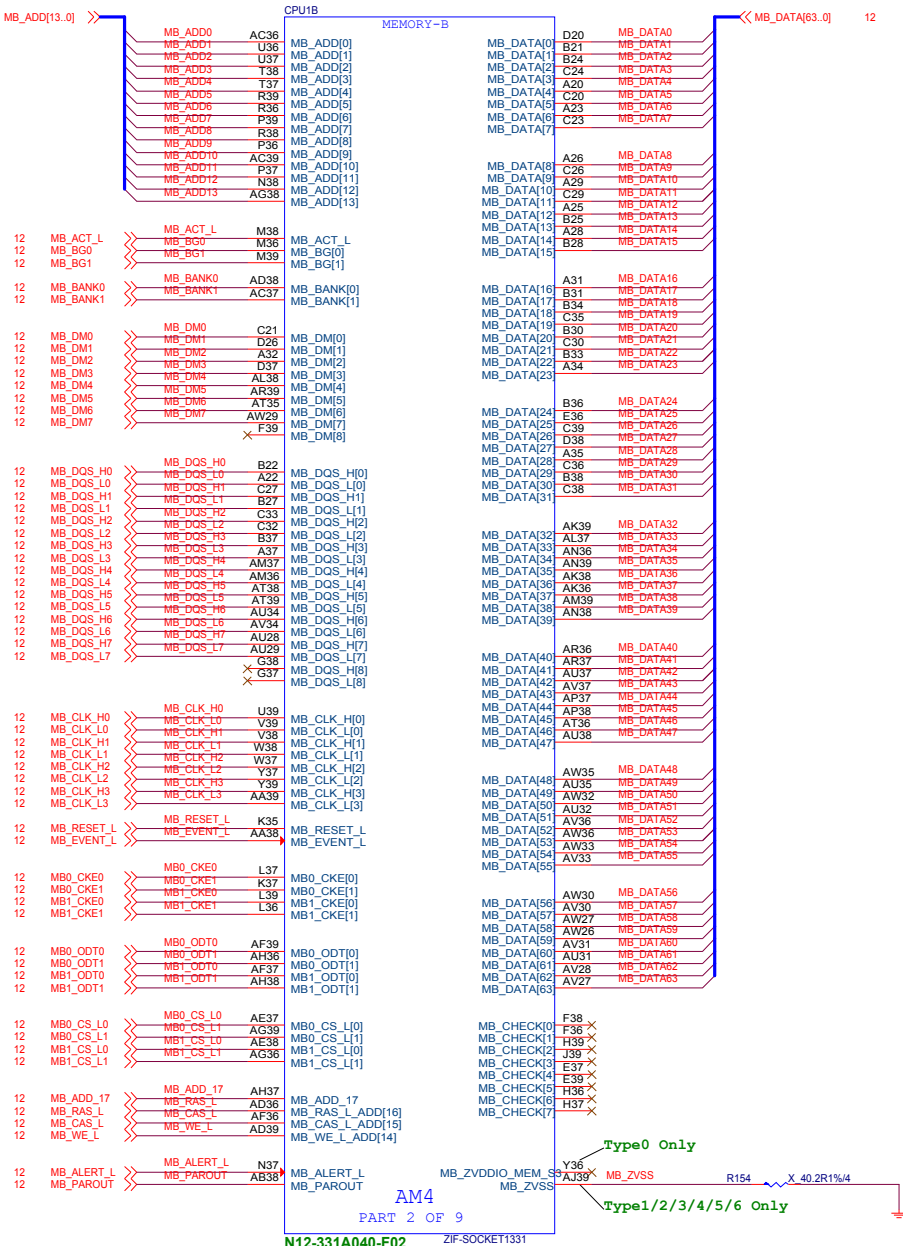
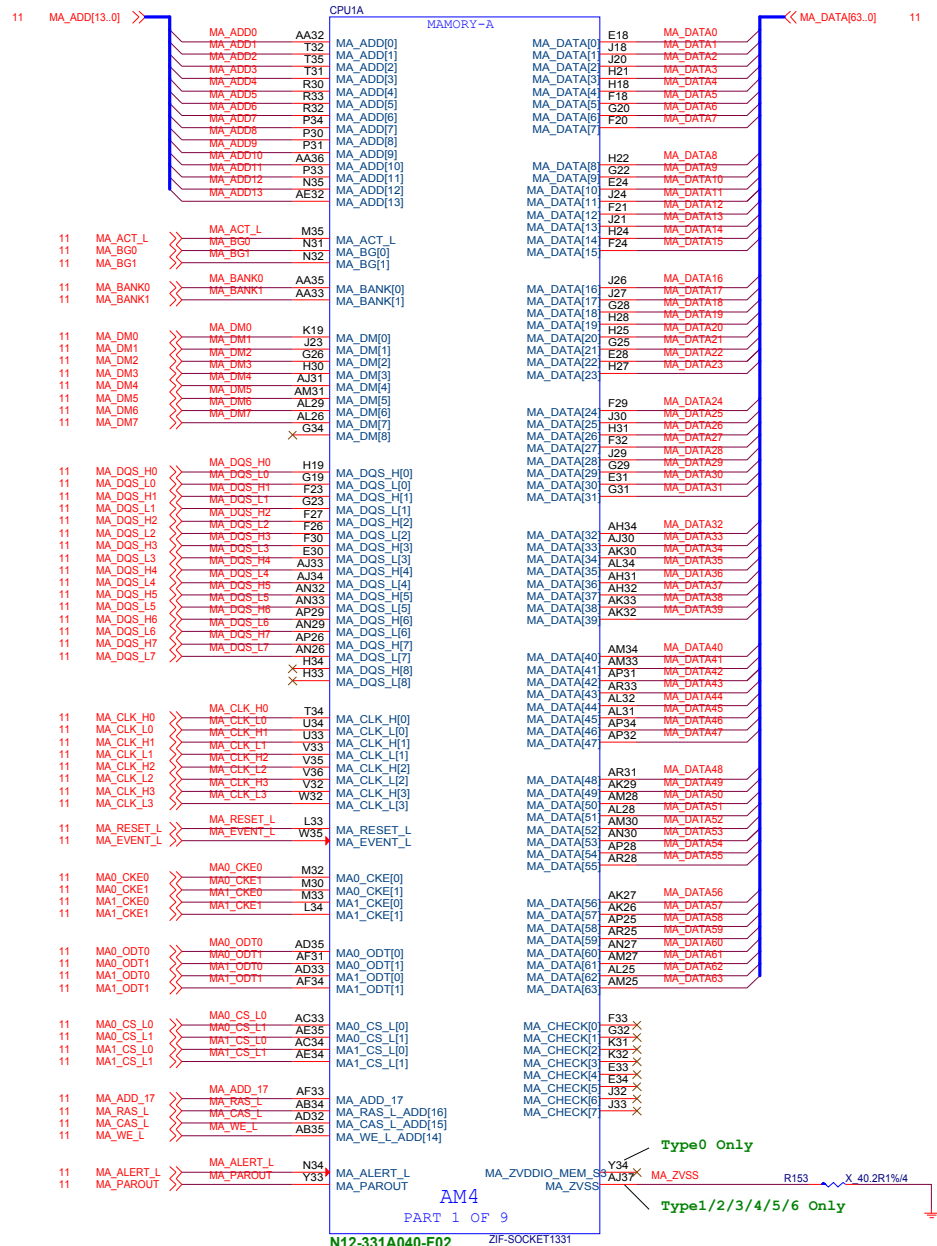
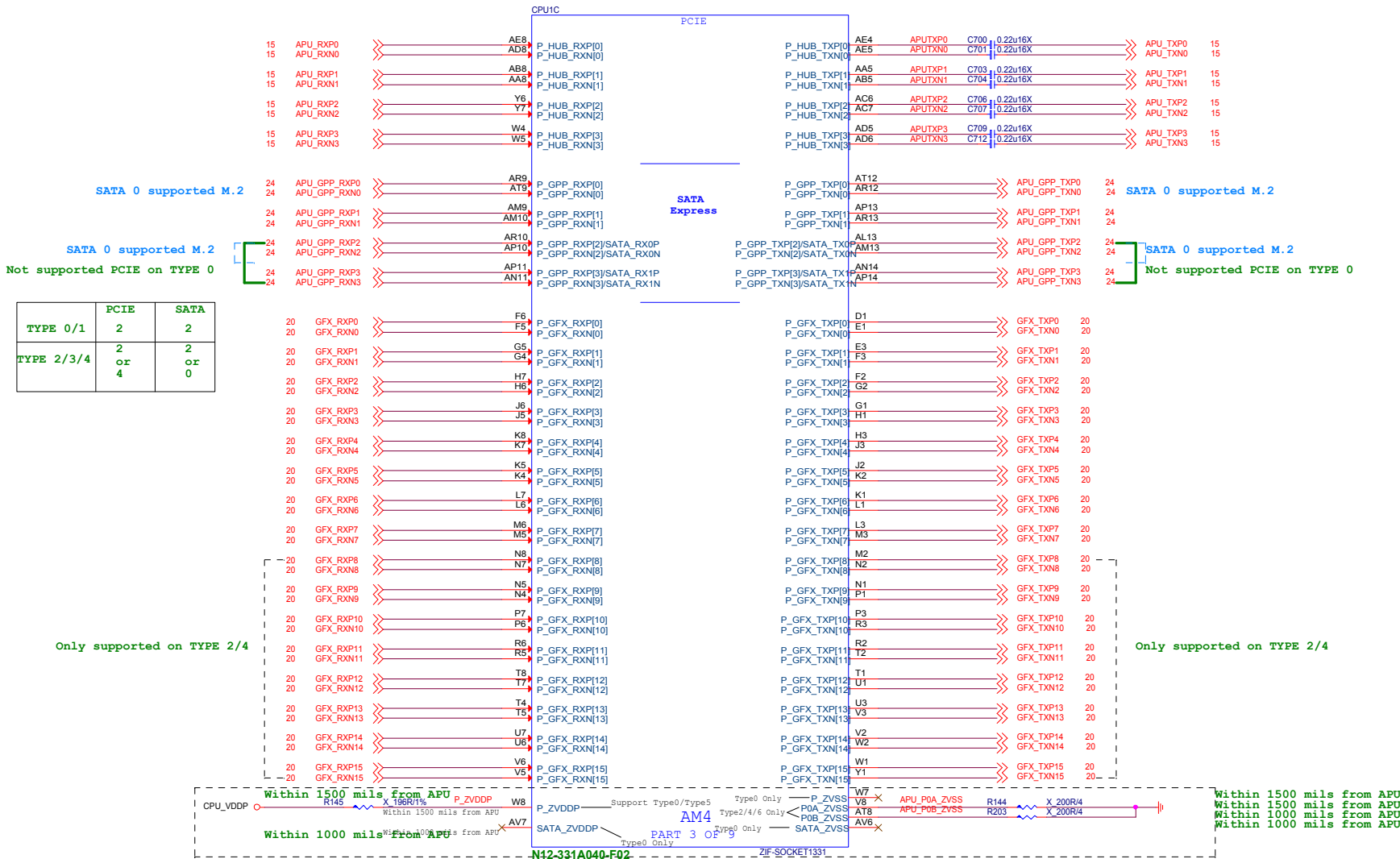


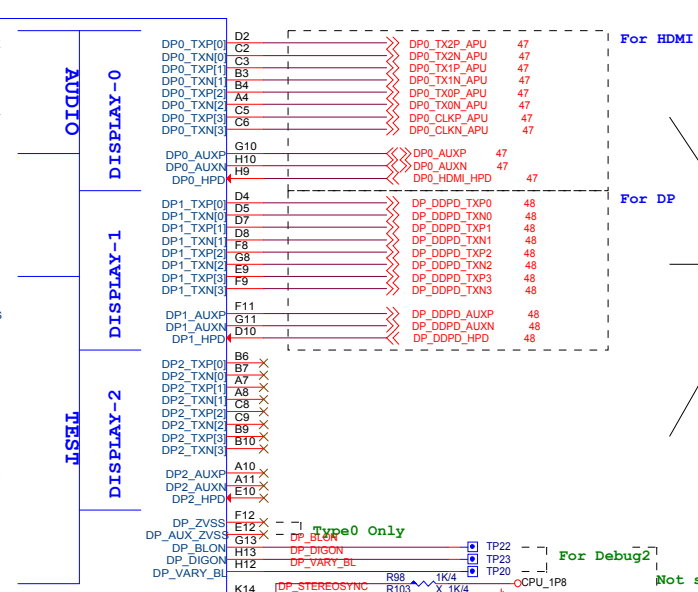
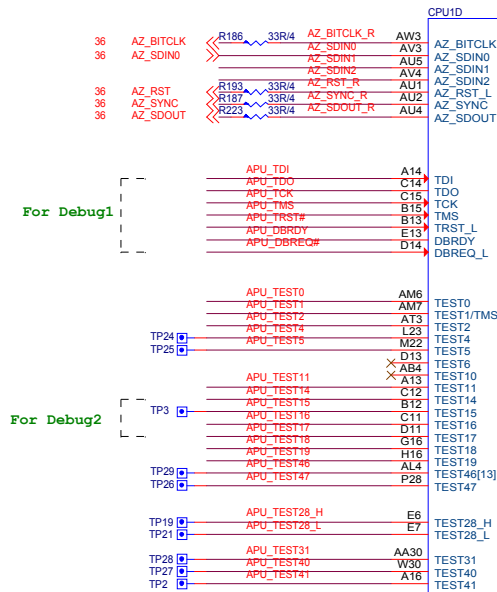
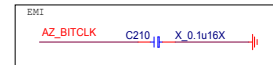
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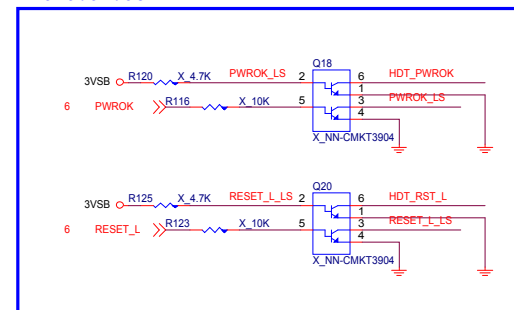
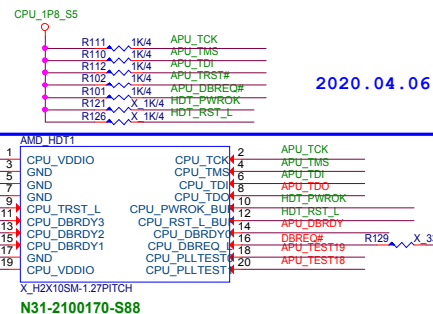
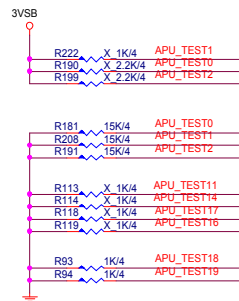


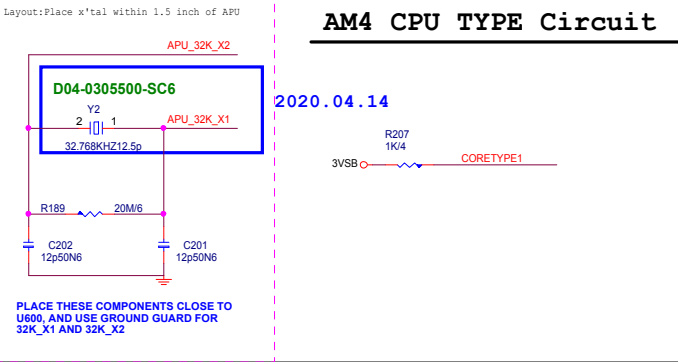
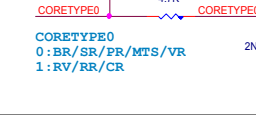
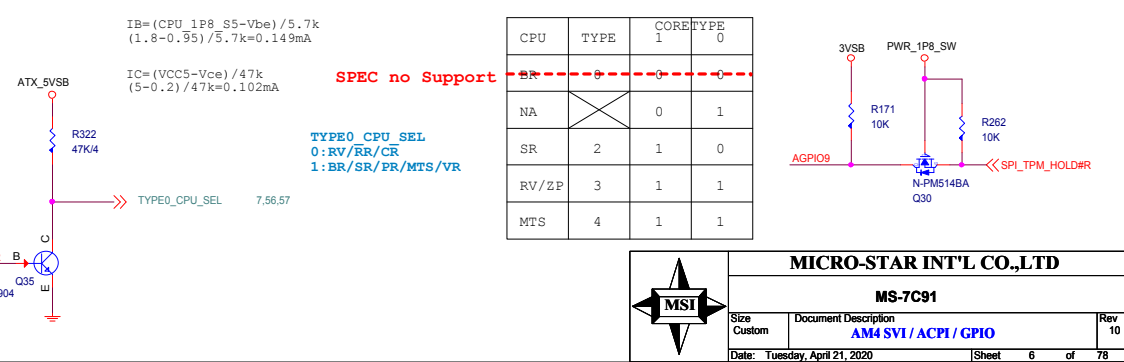
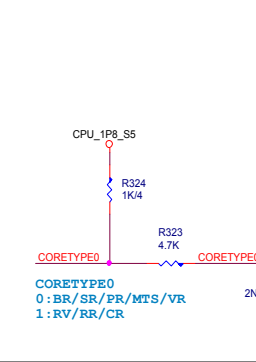
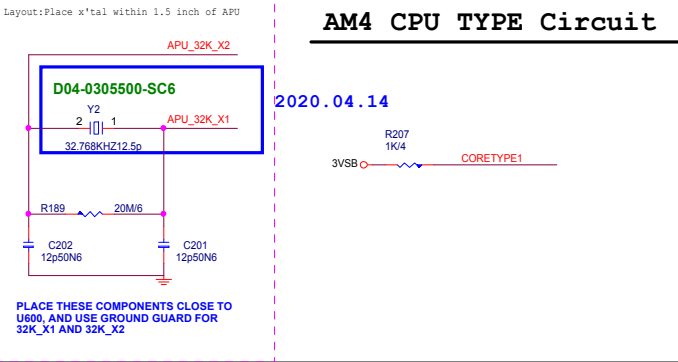
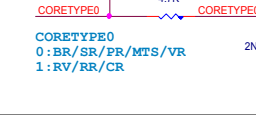
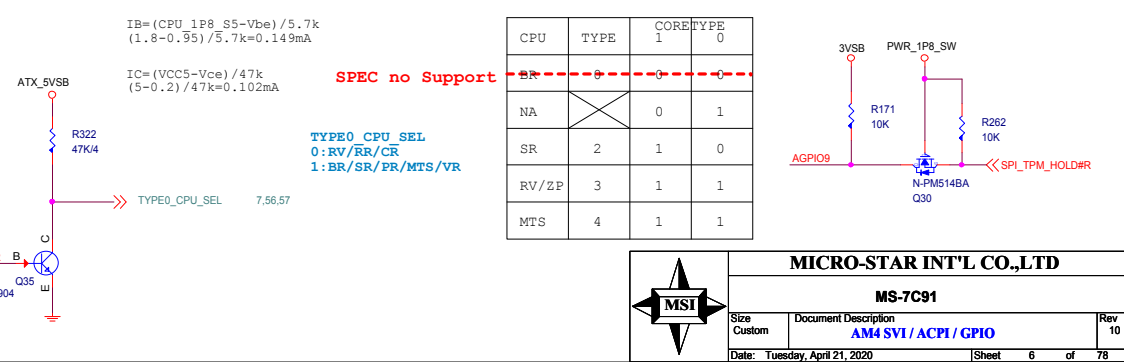
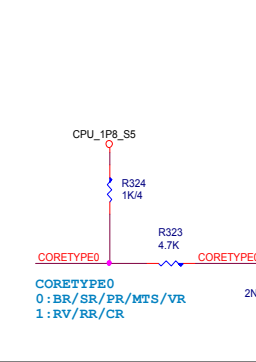
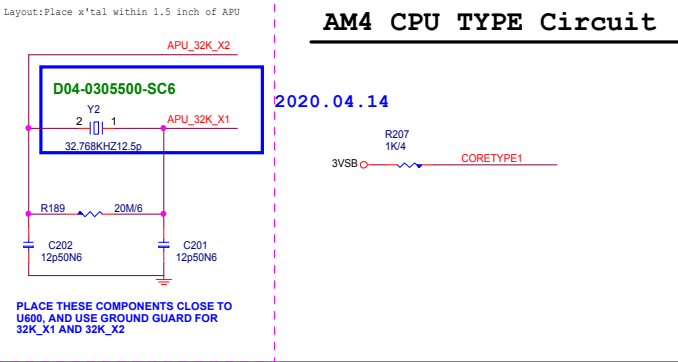
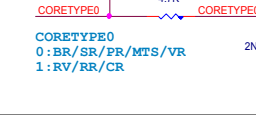
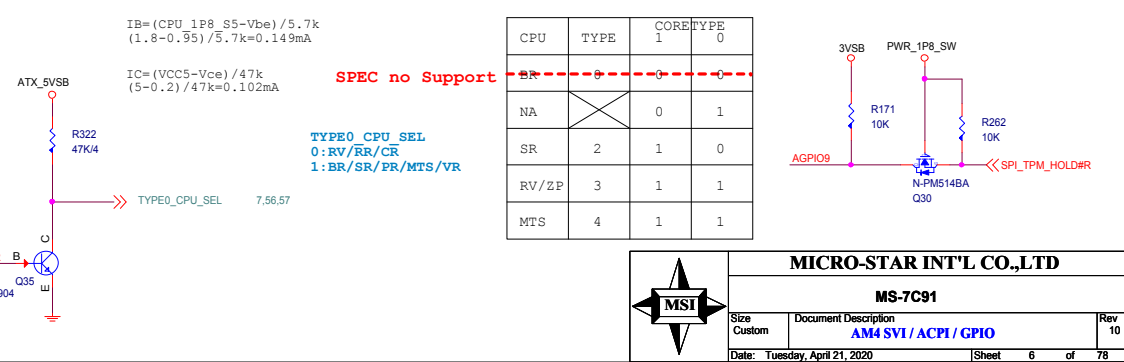
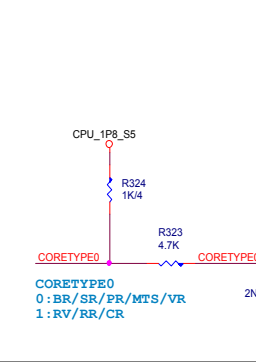
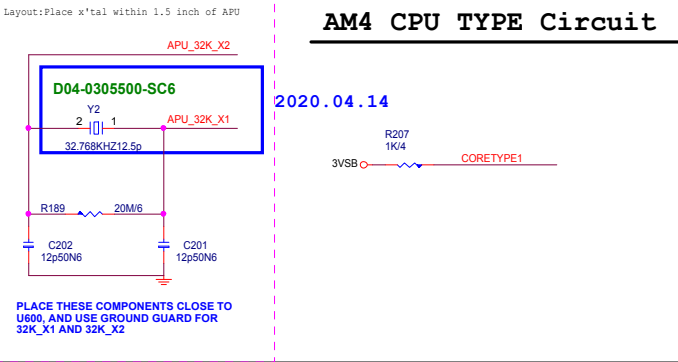
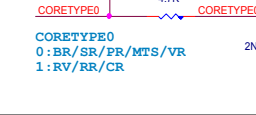
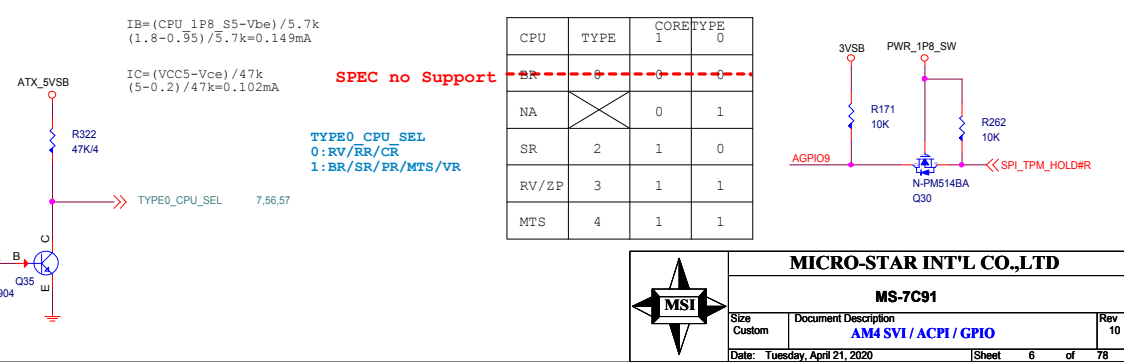
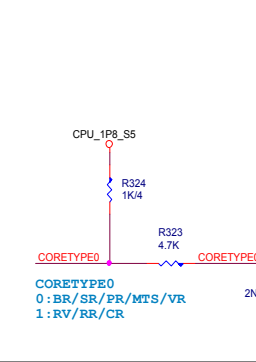
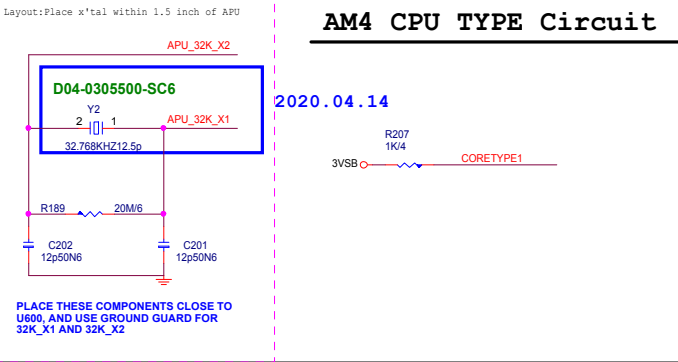
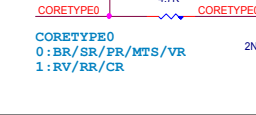
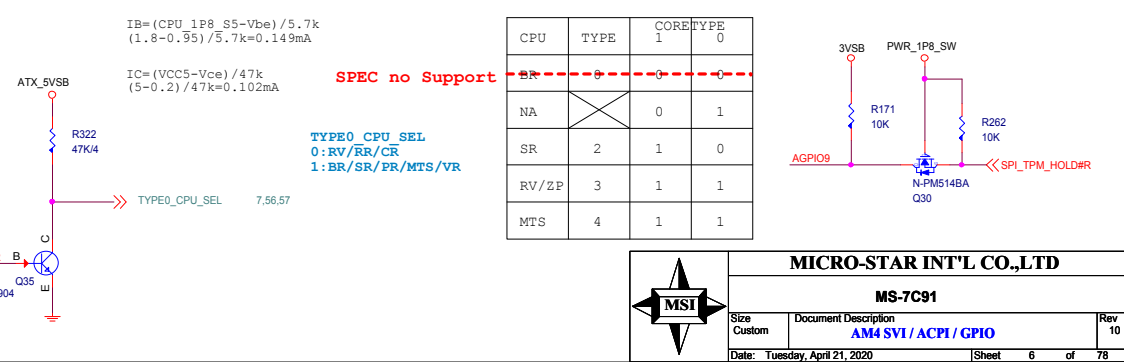
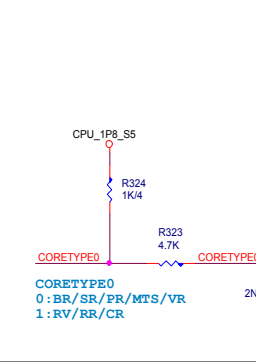
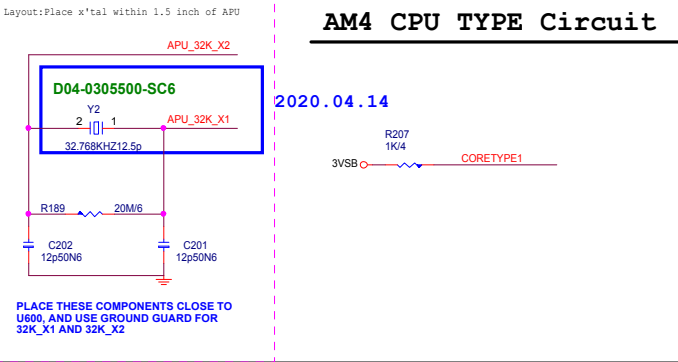
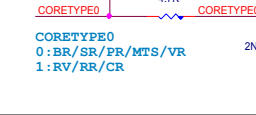
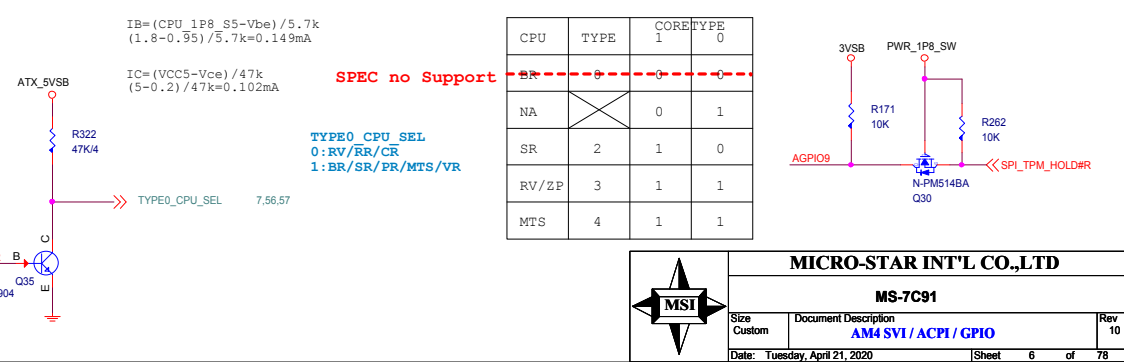
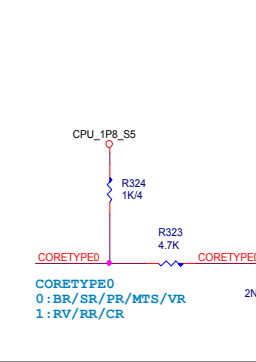
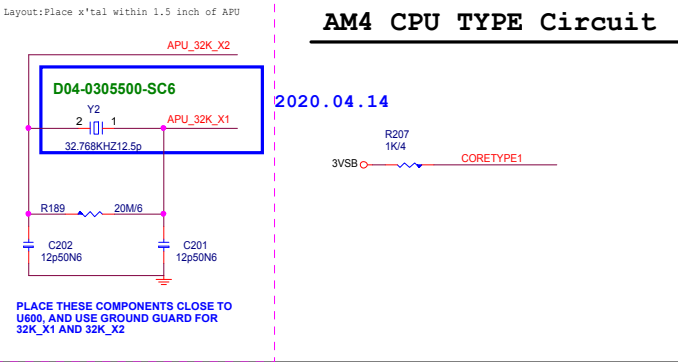
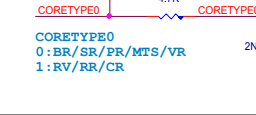
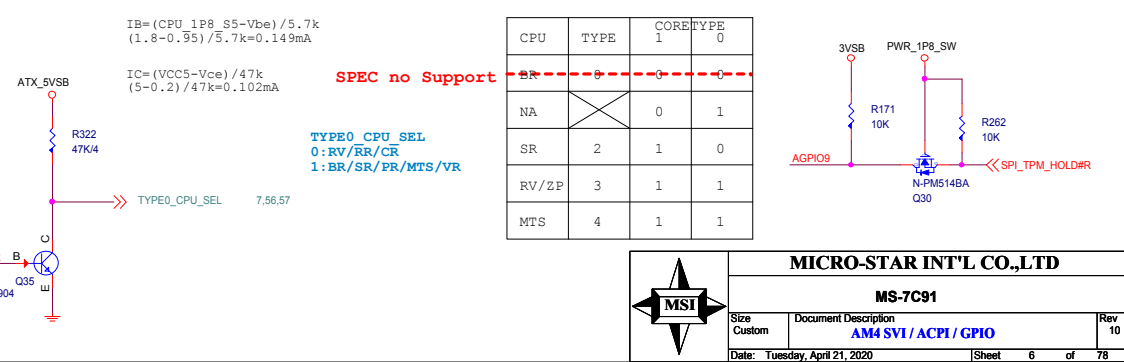
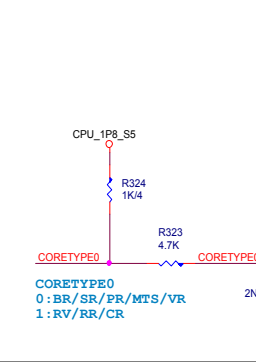
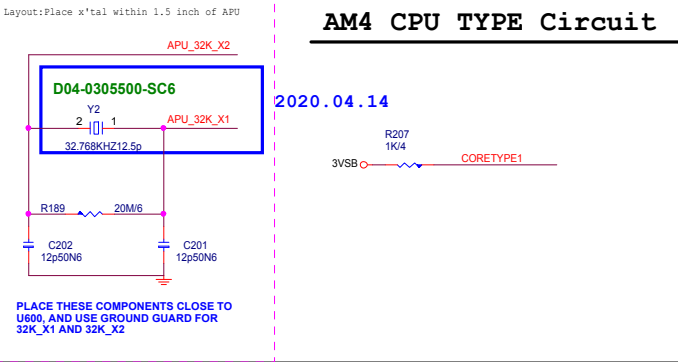
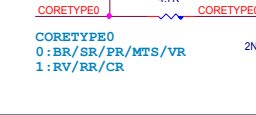
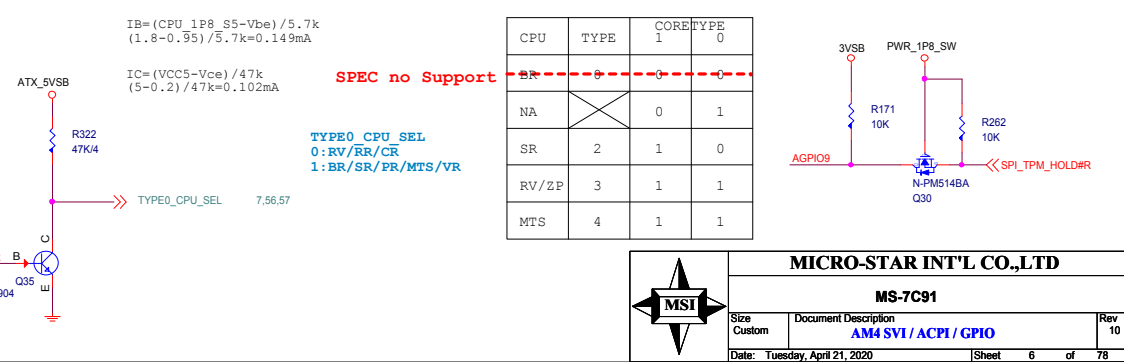
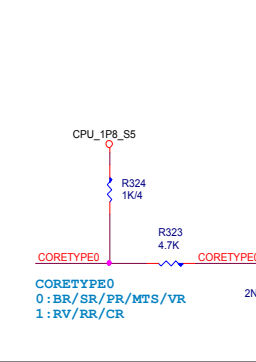
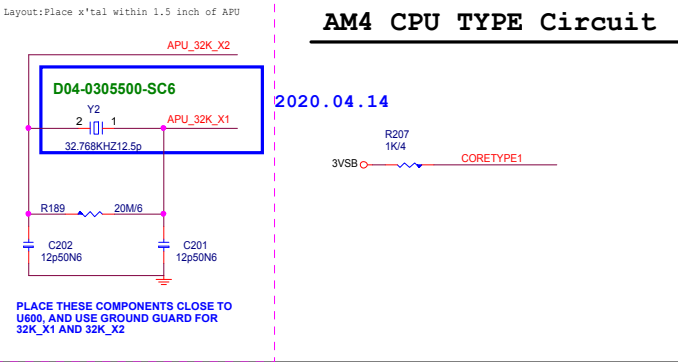
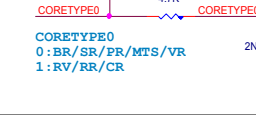
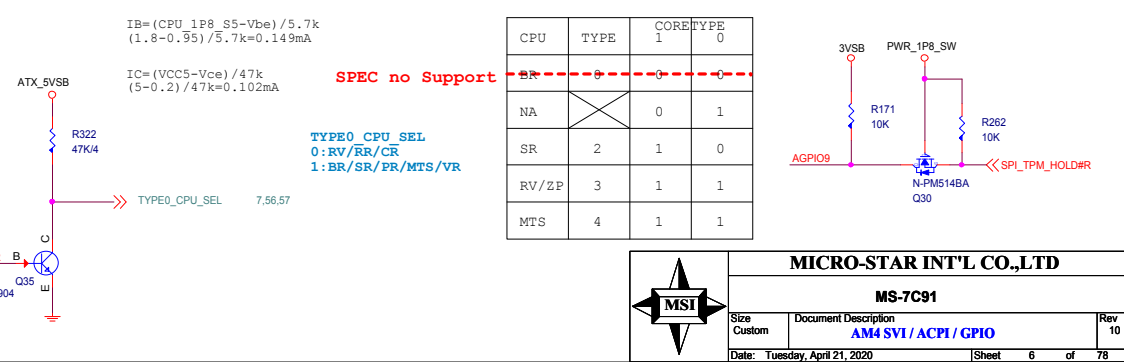
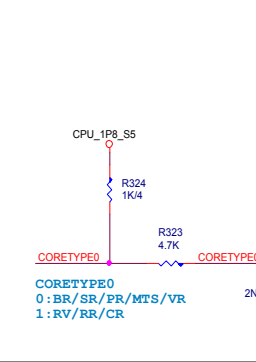
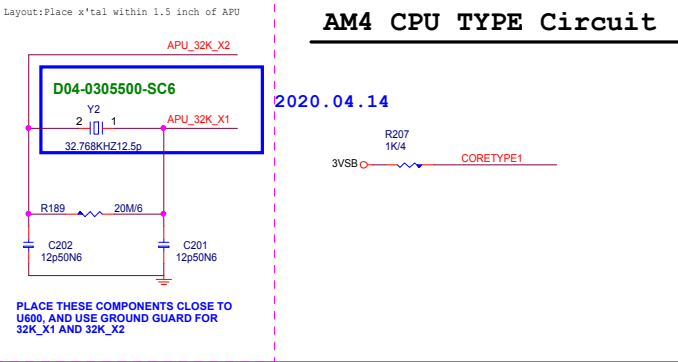
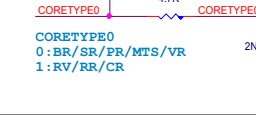
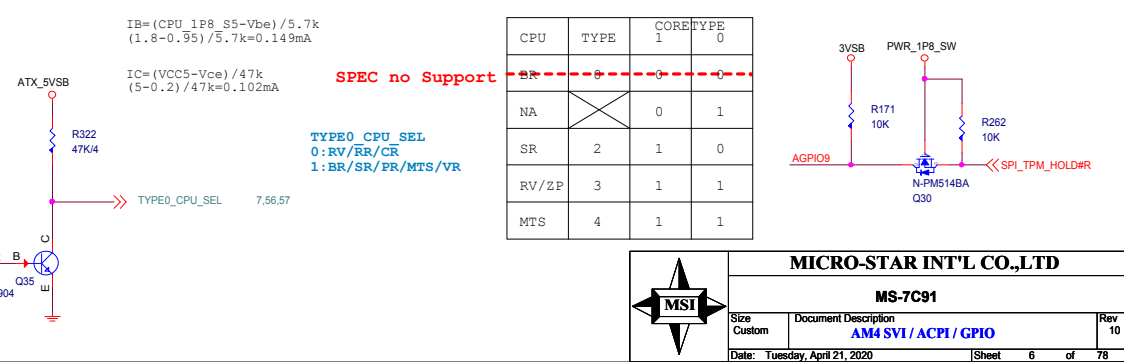
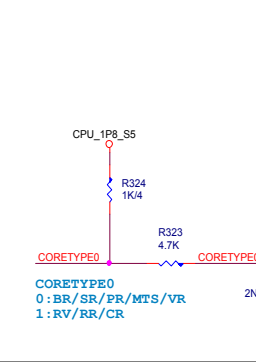
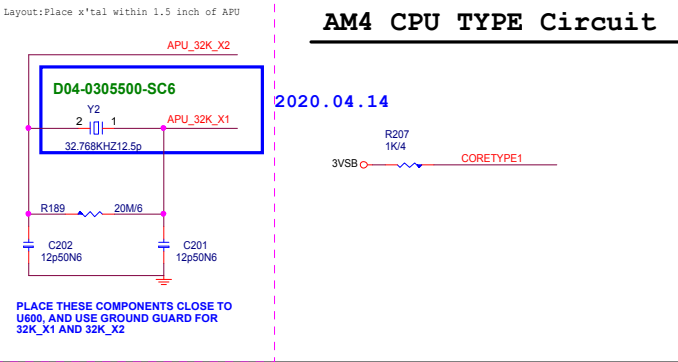
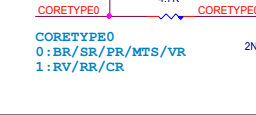
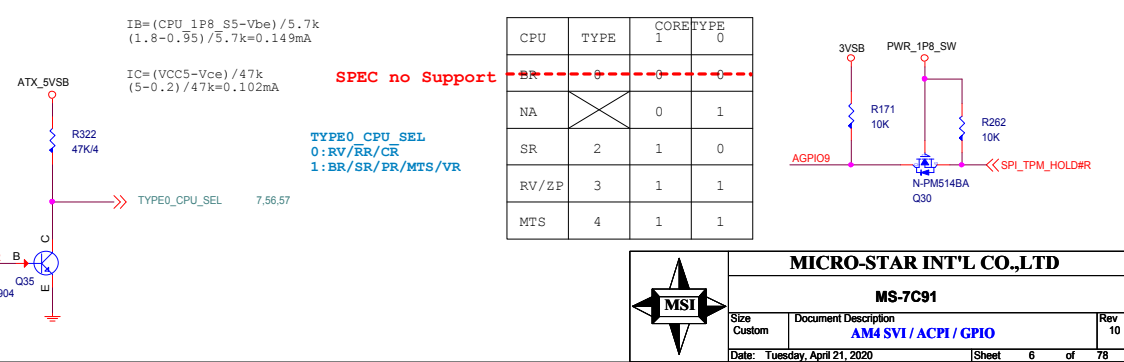
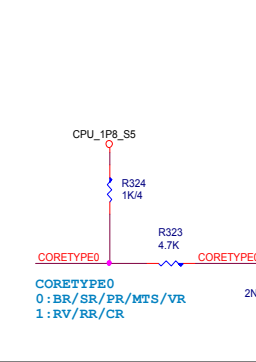
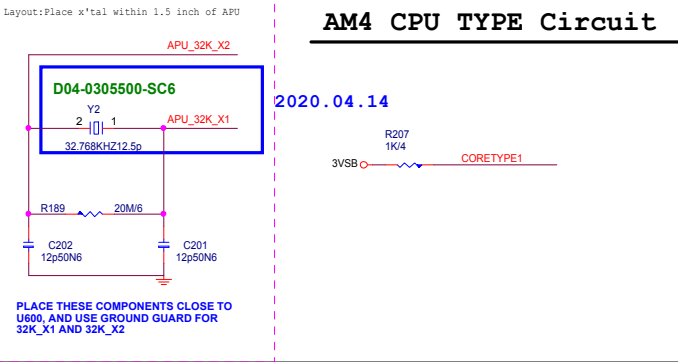
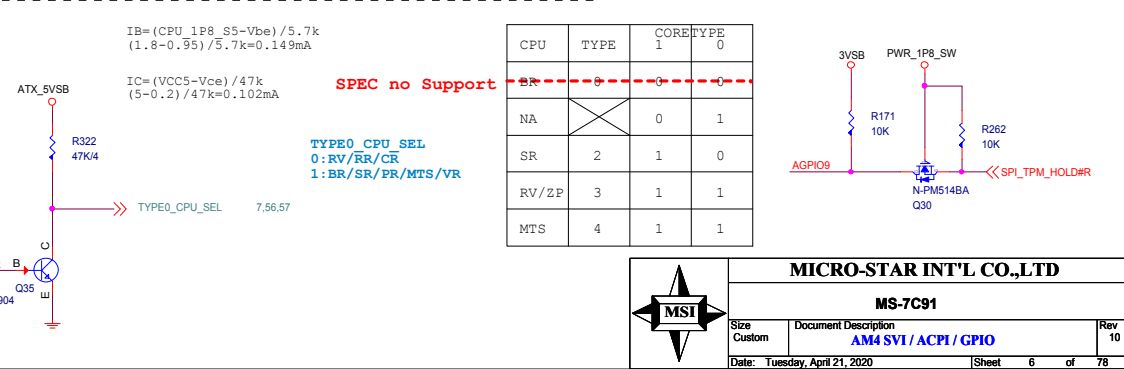
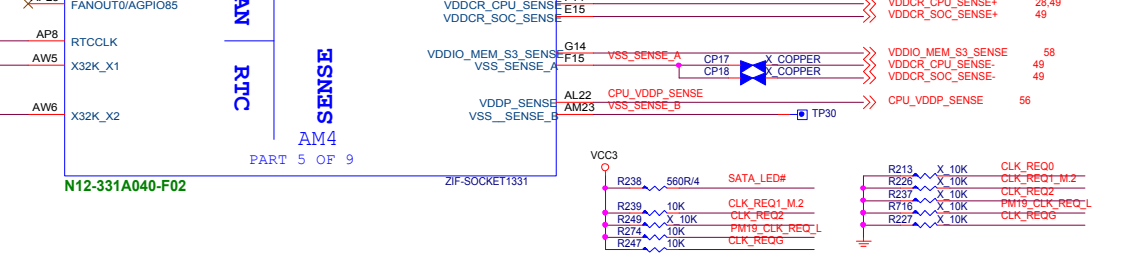
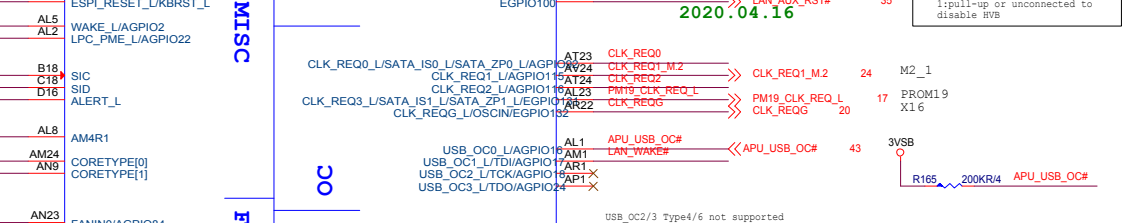
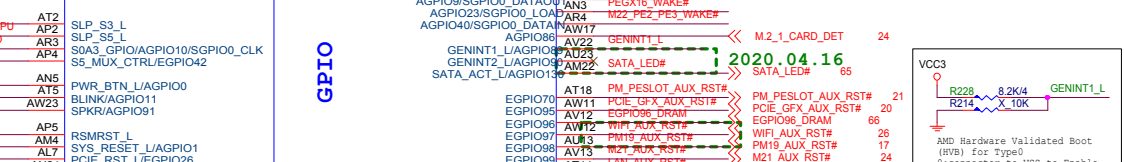
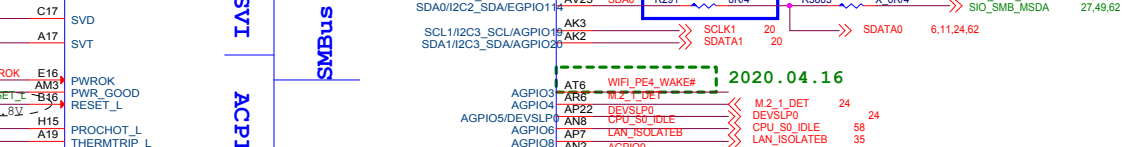
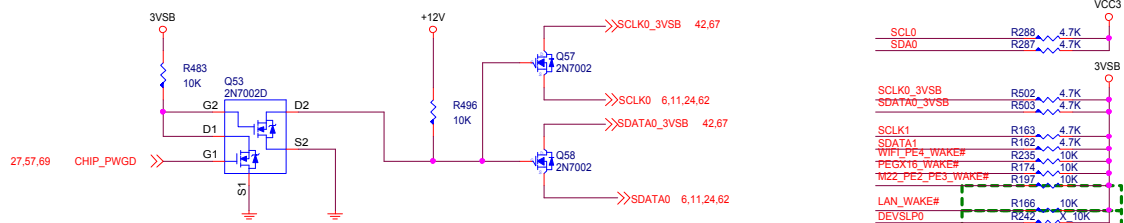
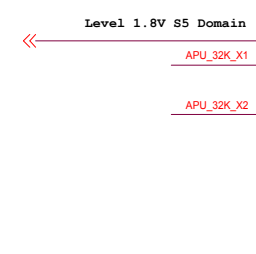
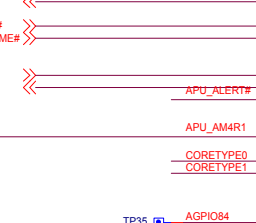
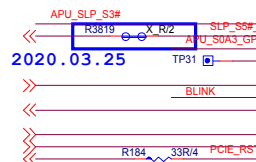
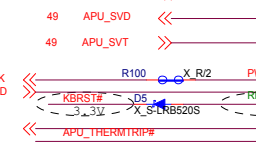
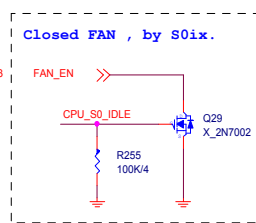
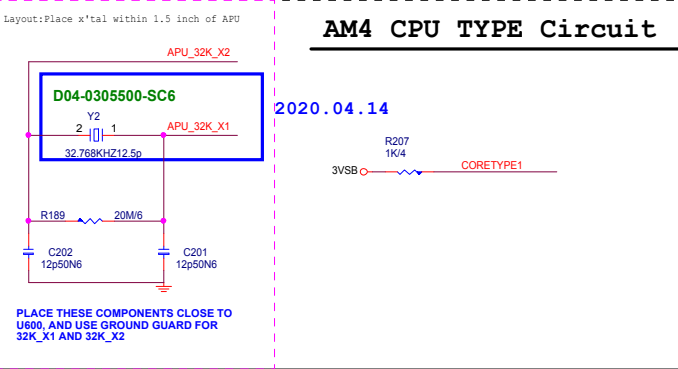
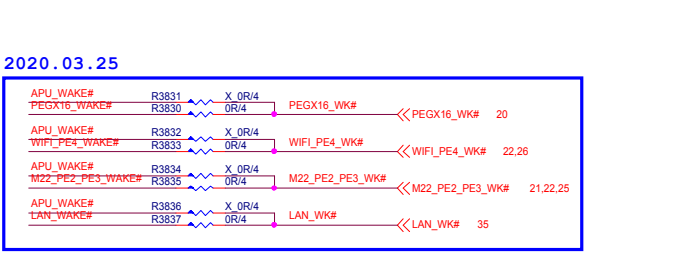
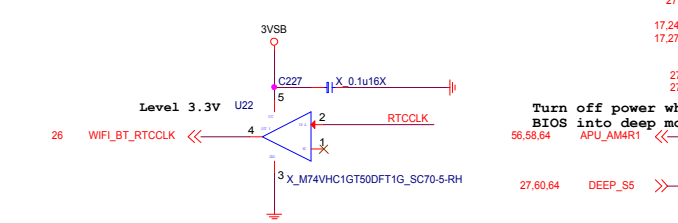
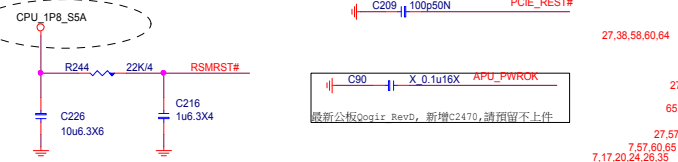
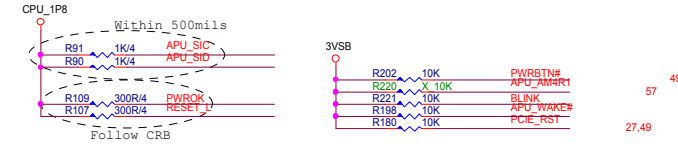
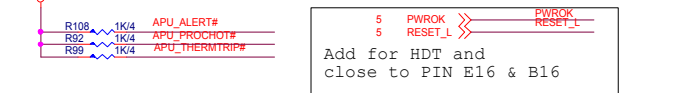
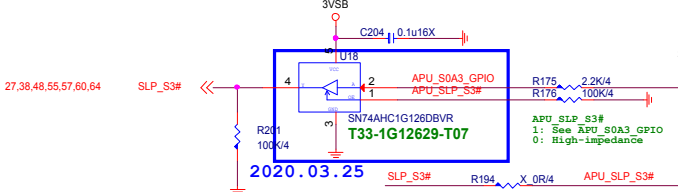




CPU\_1P8\_S5

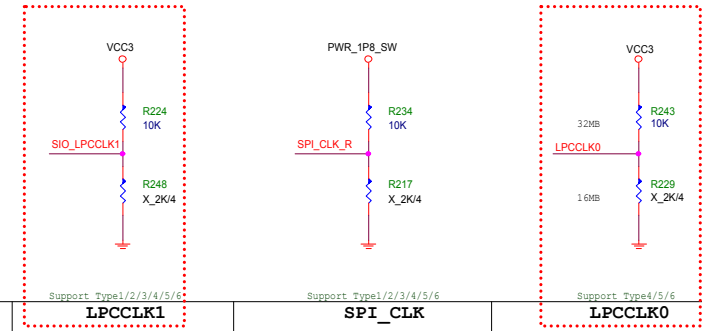
R3838 X 1K/4 APU\_TEST11



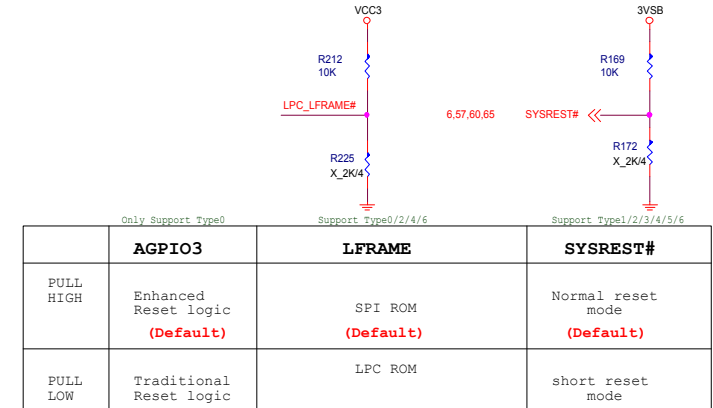




# Strapping Options

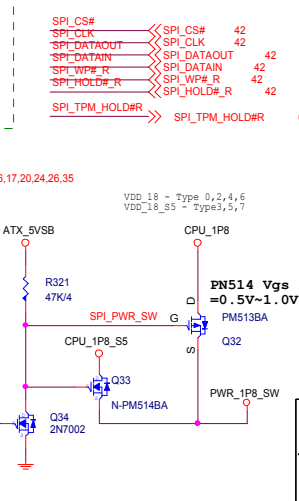
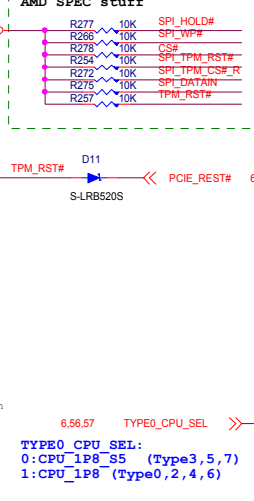
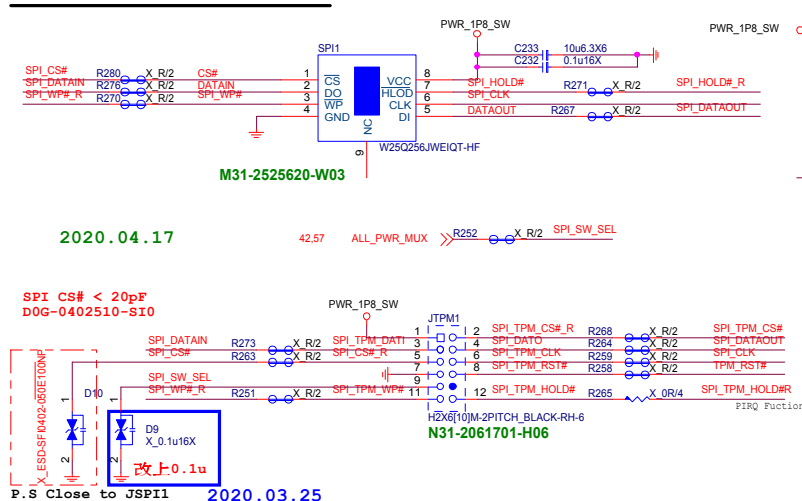


	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	PSP should modify SPI page register bits [25:24] to remap physical ROM to upper image (Default)
PULL LOW	Configured for External clock generator ????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	PSP should not modify SPI page register bits [25:24]

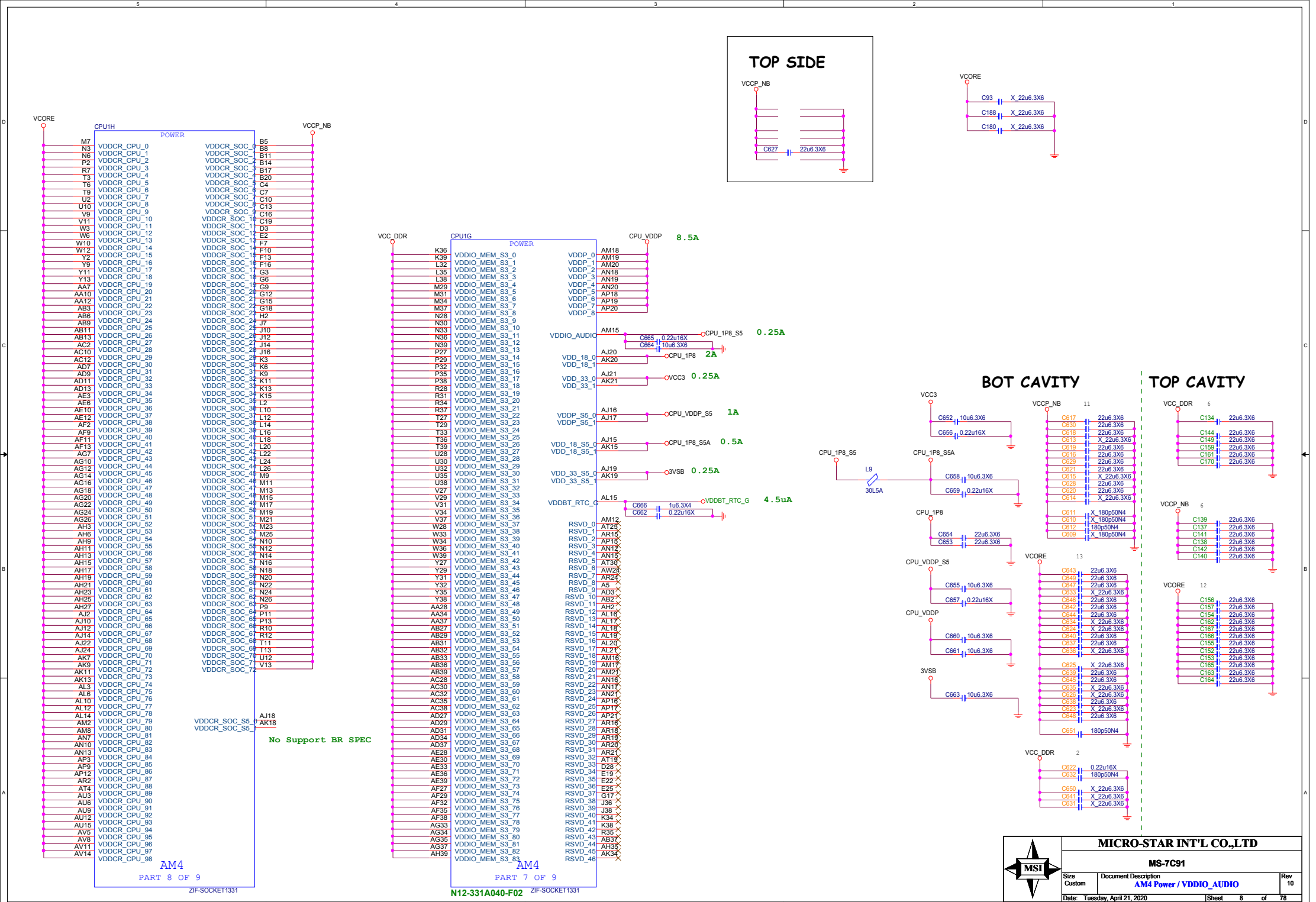


	AGPIO3	LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	SPI ROM (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	LPC ROM	short reset mode

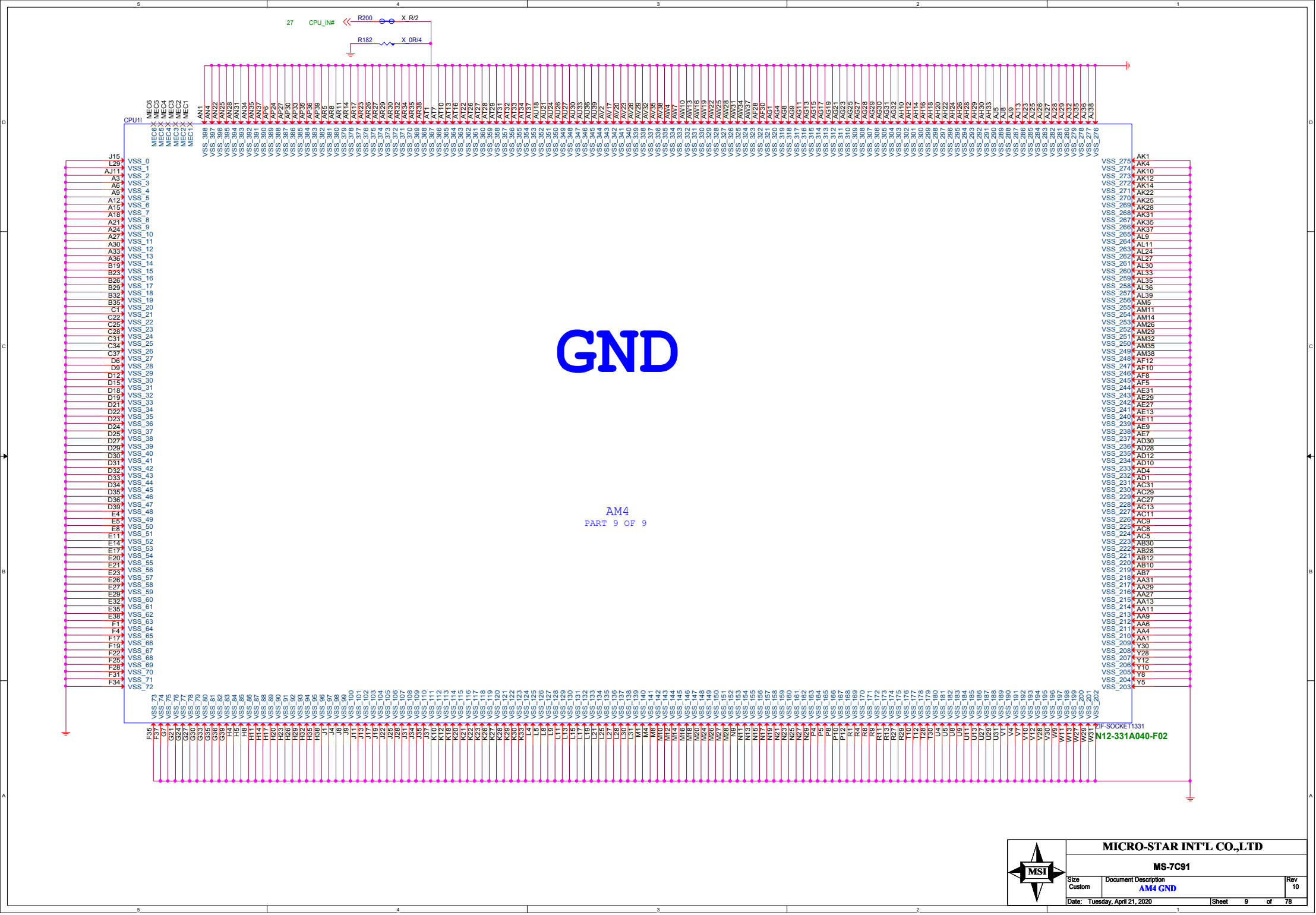
## SPI ROM(1.8V)



	RTCCCLK
PULL HIGH	RTCCCLK is input and is used as the bypass clock (Default)
PULL LOW	Normal Mode: Use 32Khz xtal as the source of RTC clock







**MICRO-STAR INT'L CO.,LTD**

MS-7C91

Size	Custom
------	--------

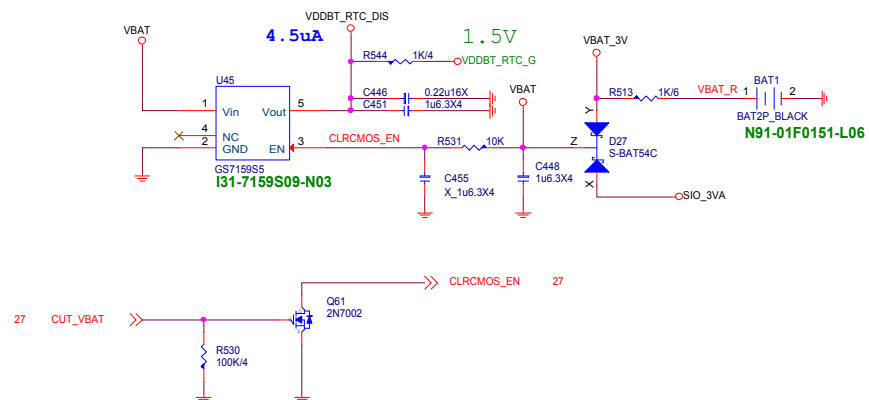
Document Description	AM4 GND
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Rev  
10

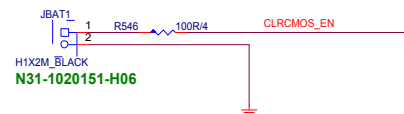
Date: Tuesday, April 21, 2020

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## RTC & Clear CMOS Circuit



### Clear CMOS button



**MICRO-STAR INT'L CO.,LTD**

MS-7C91

Size  
Custom

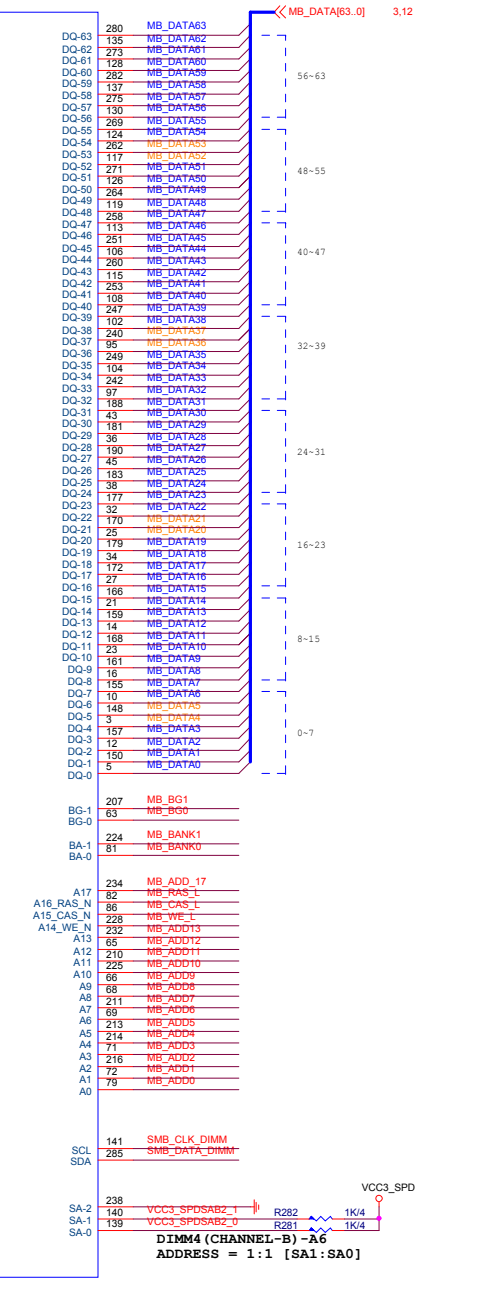
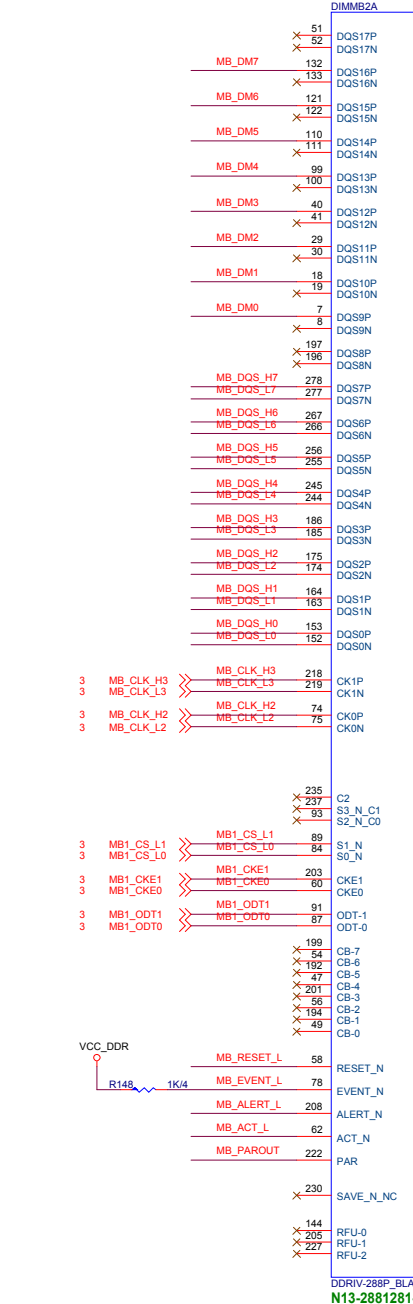
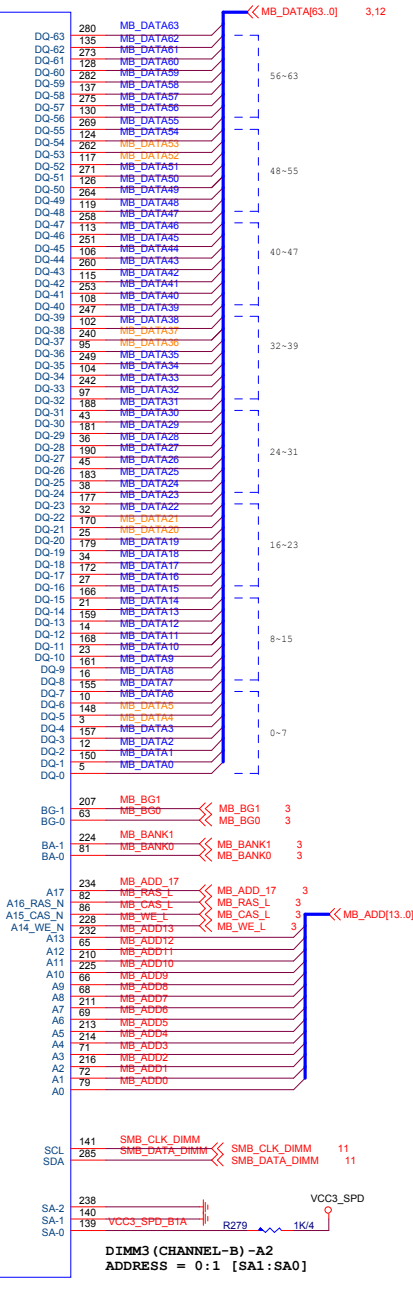
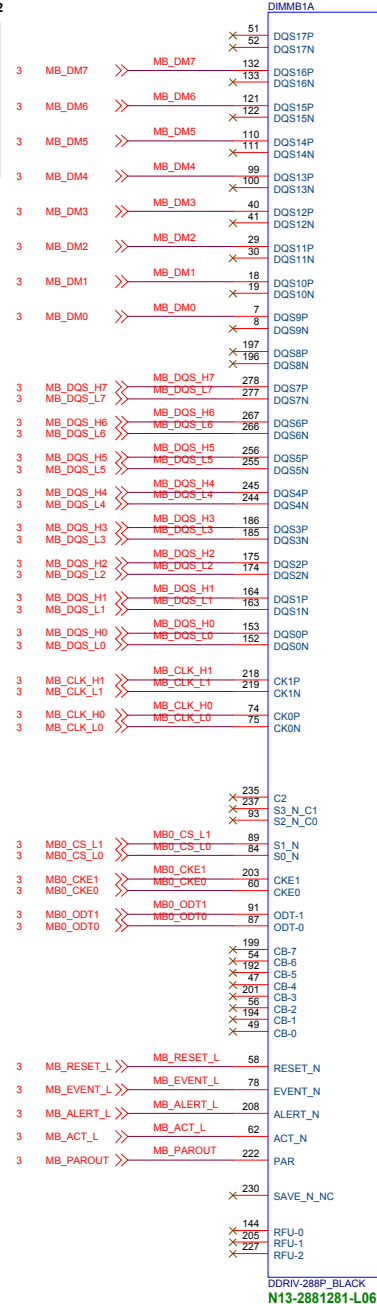
Document Description
<b>RTC / CMOS</b>

Rev	10
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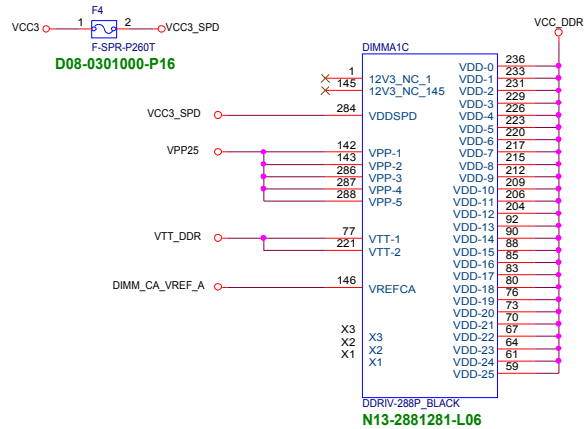
Date: Tuesday, April 21, 2020

Sheet	10	of	78
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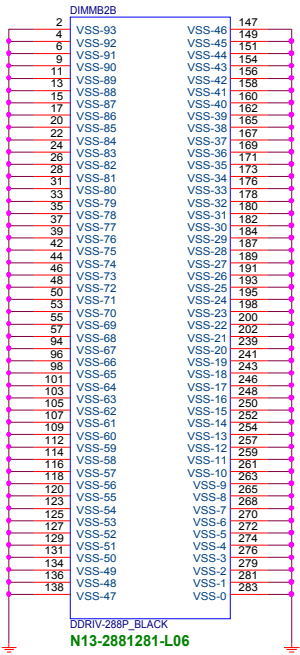
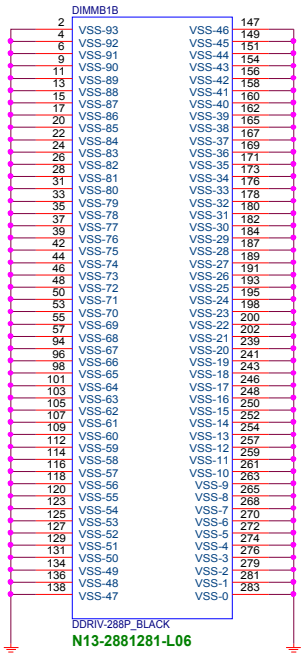
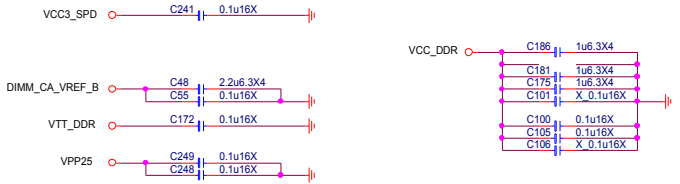
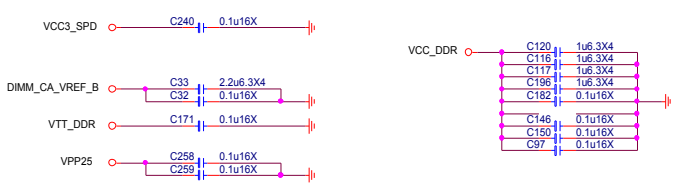
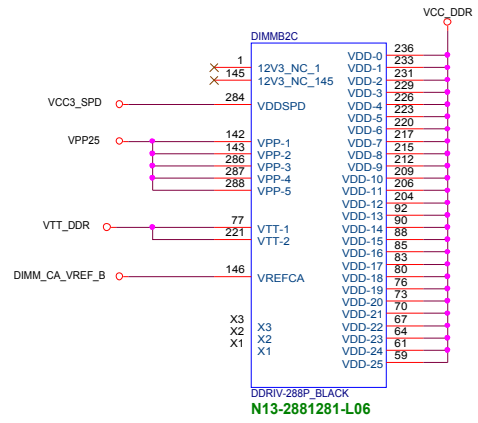
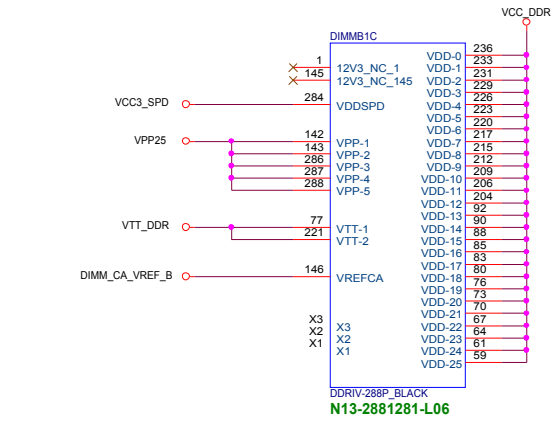
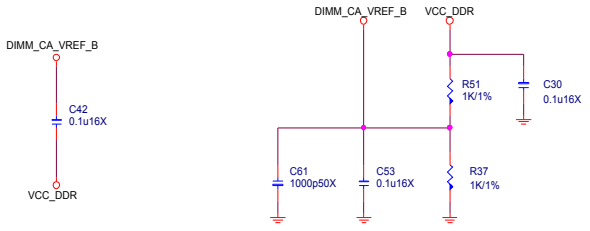




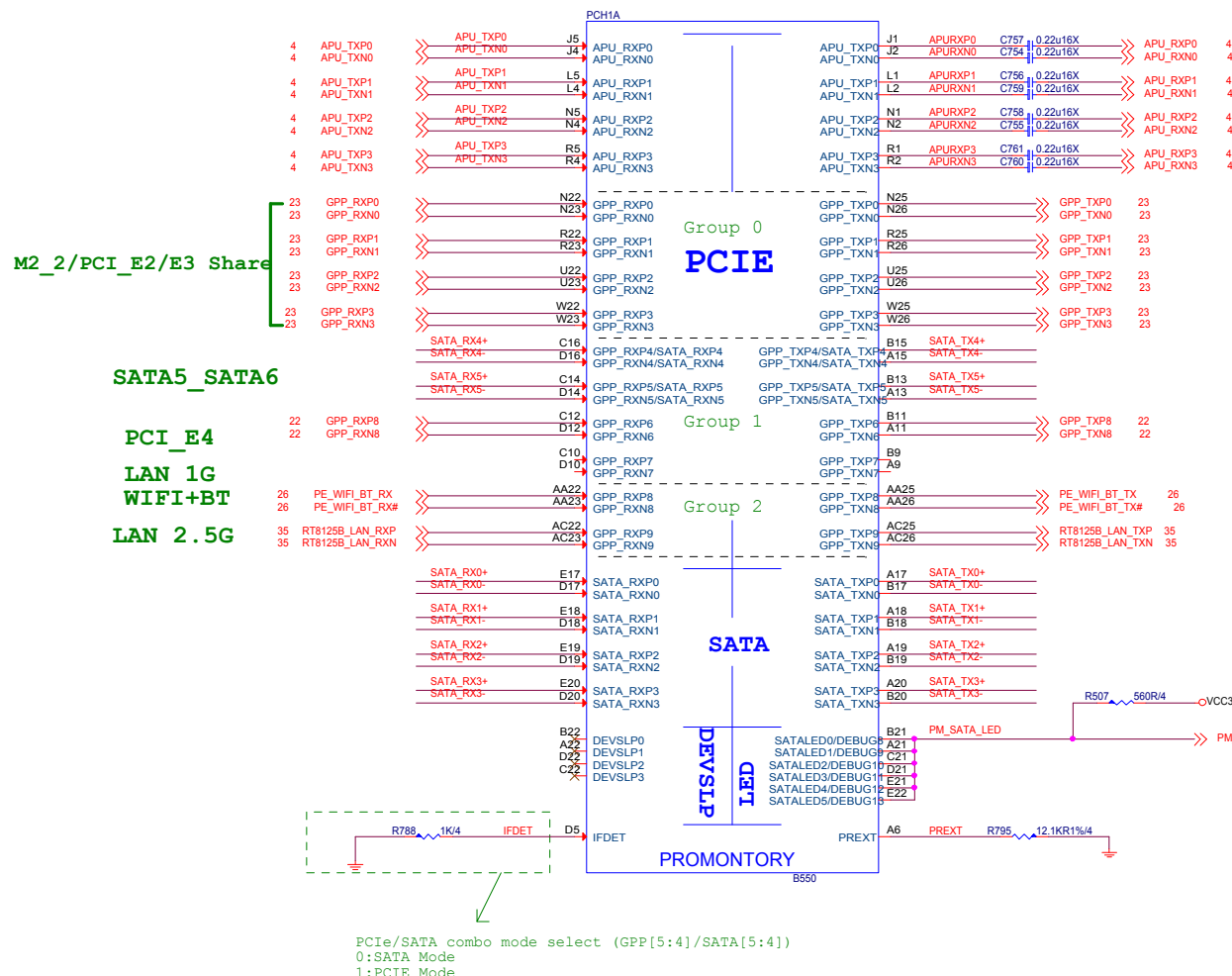
av1:D08-0301100-B07



DDR VREF  
(place resistors close to DIMMs)

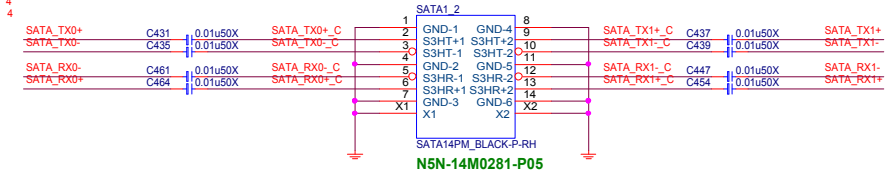




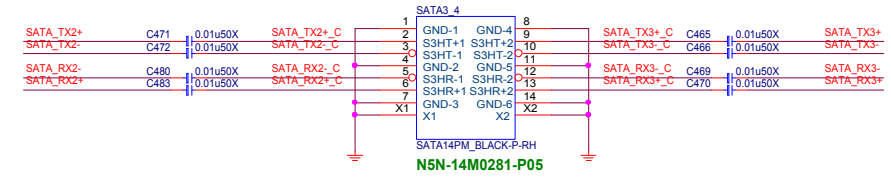


## SATA Connector

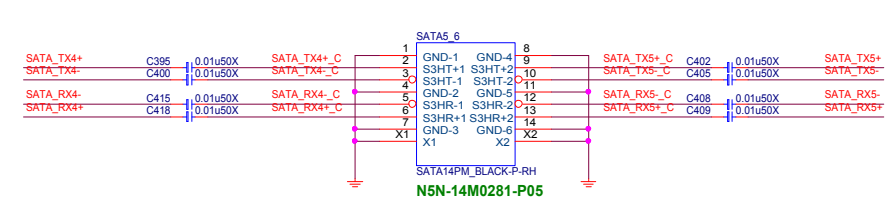
### SATA1\_2



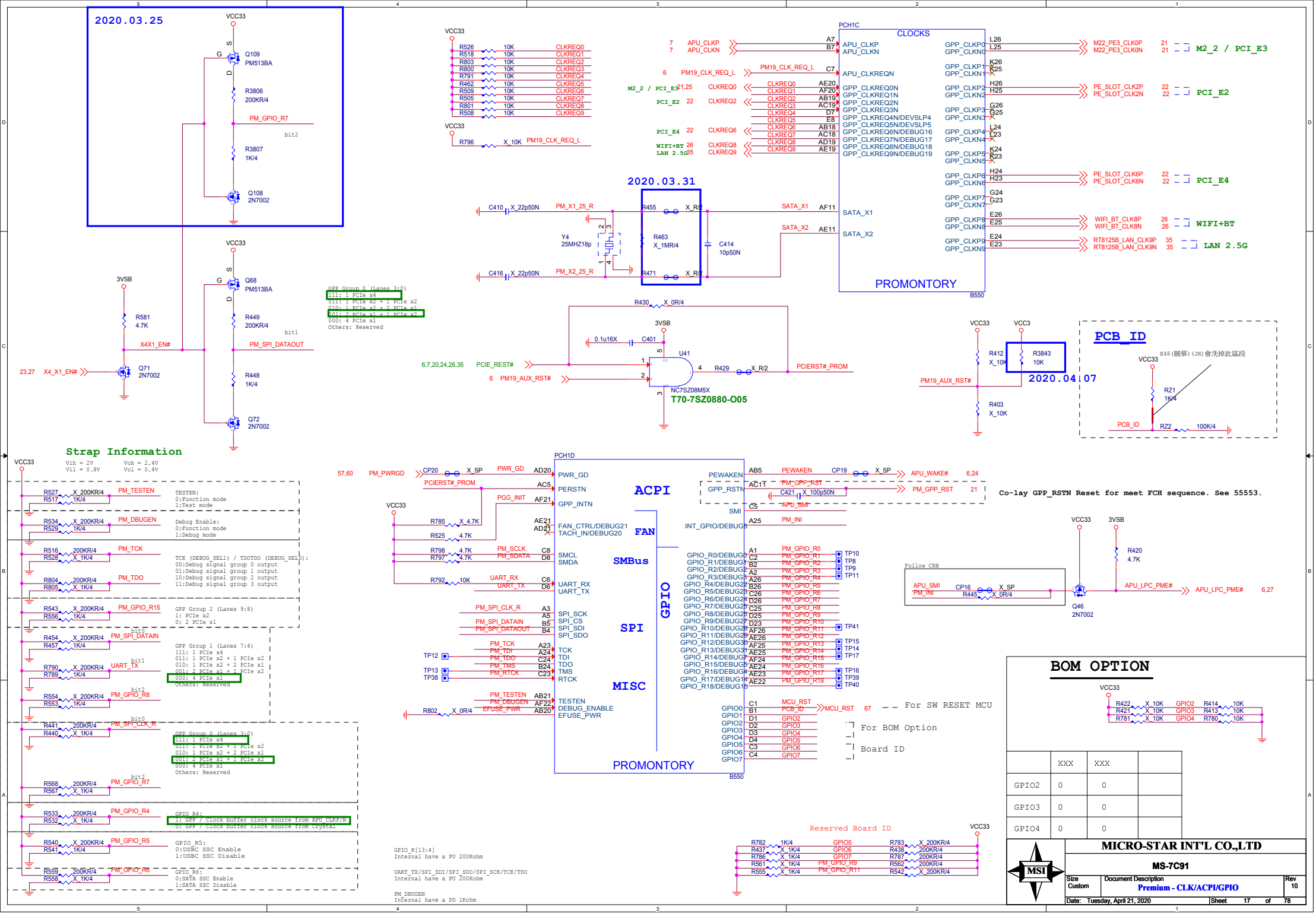
### SATA3\_4

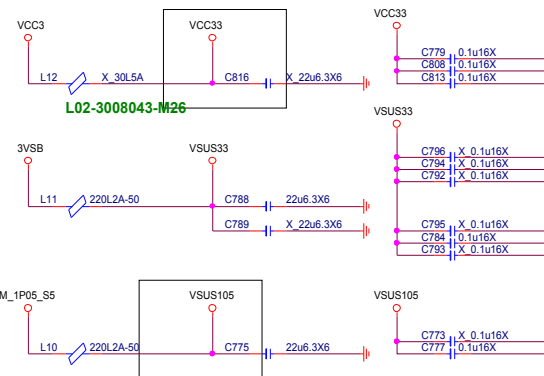
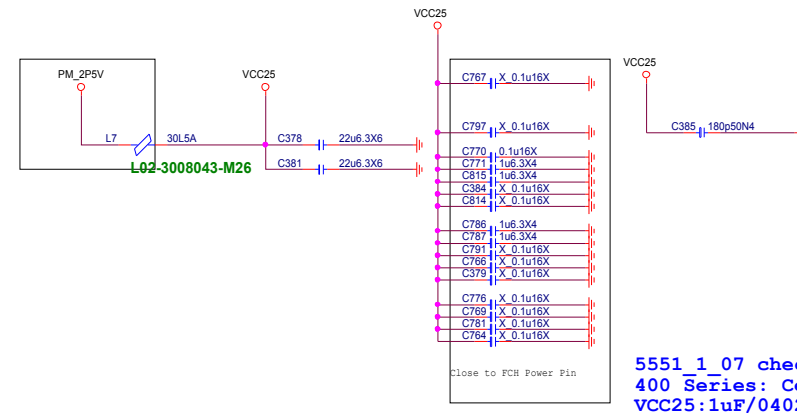
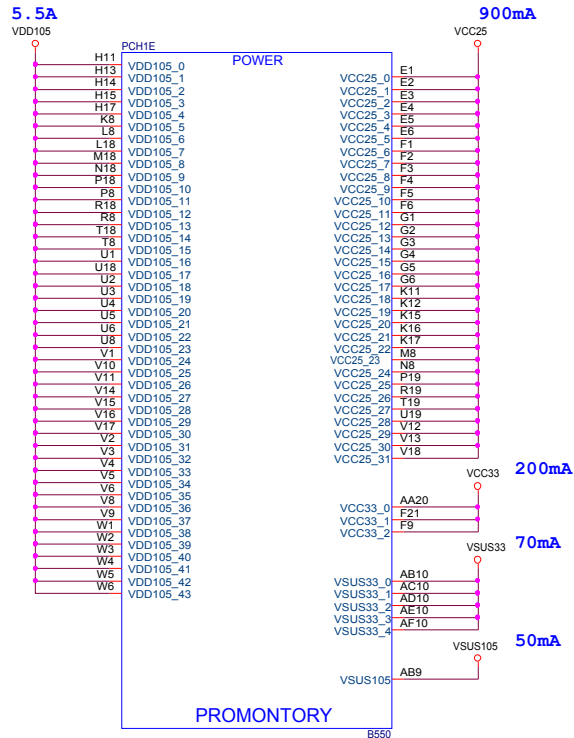
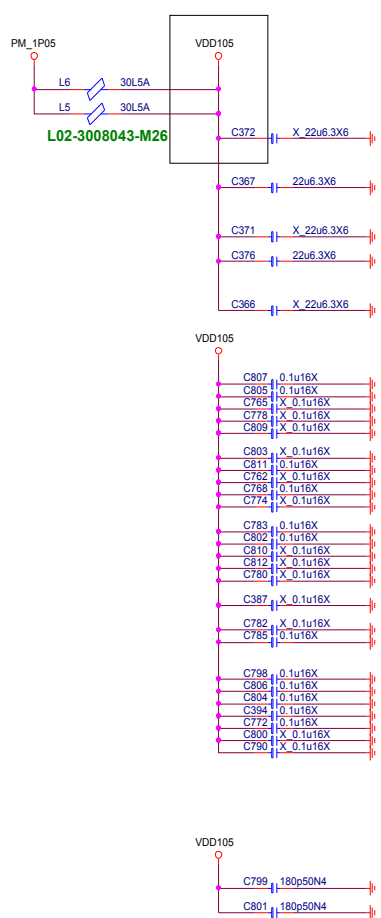


### SATA5\_6

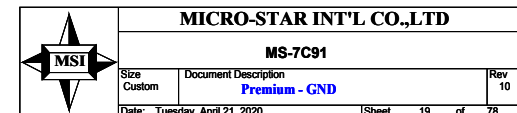






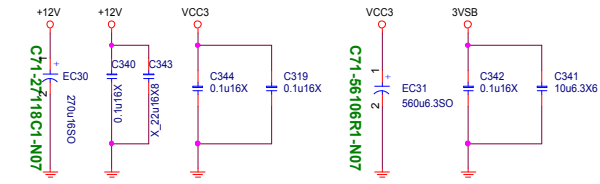
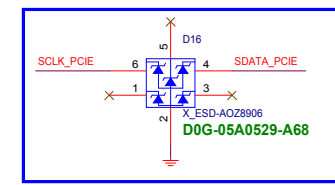
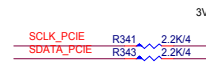


5551\_1\_07 check list  
400 Series: Ceramic capacitors.  
VCC25:1uF/0402

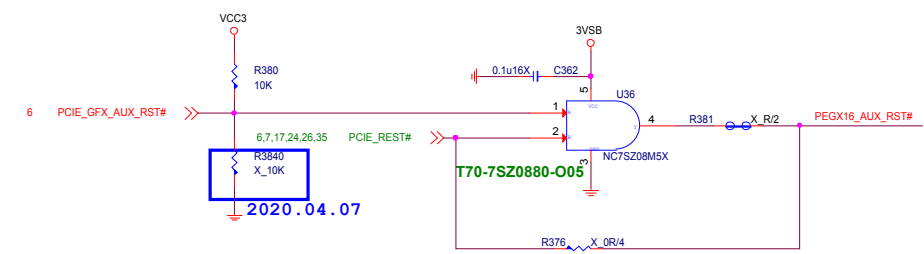
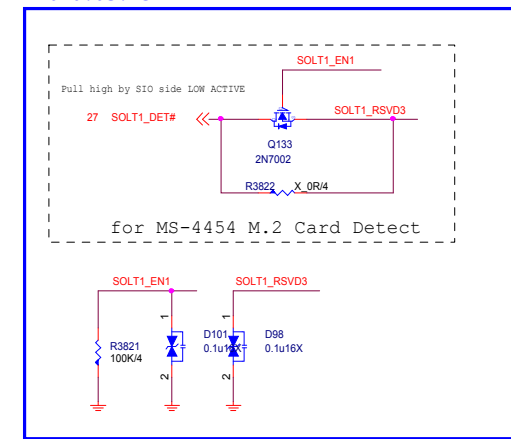


PCI\_E1

SMB\_SEL  
GPIO Default High



2020.03.25



+12V		- 5.5 A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

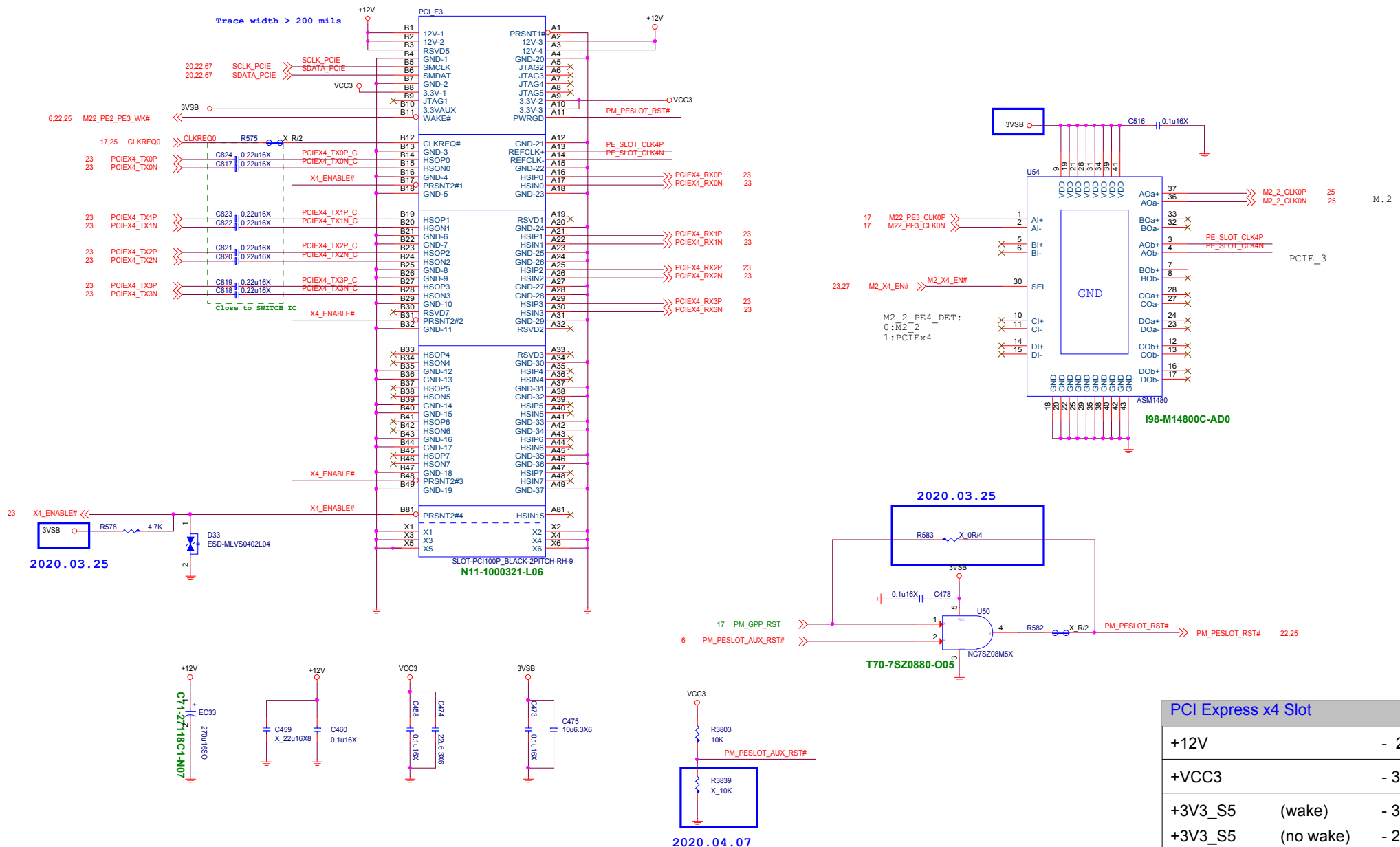


Size Custom	Document Description <b>PCI_E2 (X16)</b>	Rev 10
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**PCI EXPRESS x4 SLOT**

PCI\_E3 X4



PCI Express x4 Slot		
+12V		- 2.1A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA



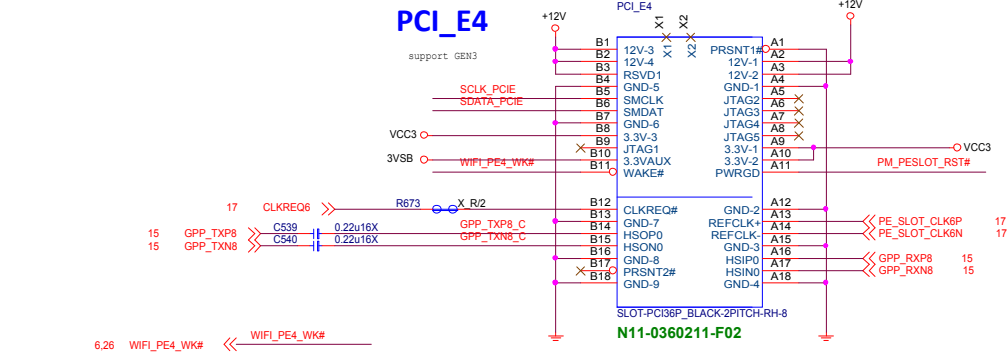
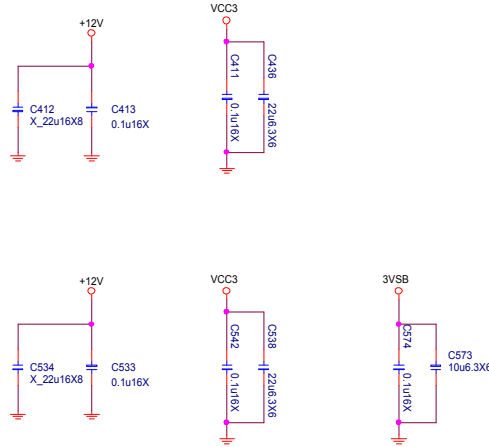
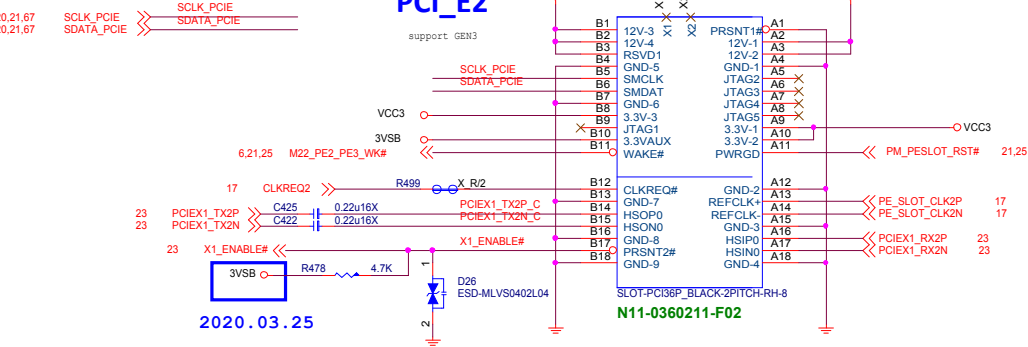
**MICRO-STAR INT'L CO.,LTD**

MS-7C91


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PCI EXPRESS X1 SLOT

20.21.67 SCLK\_PCIE  
20.21.67 SDATA\_PCIE



PCI Express x1 Slot *3	
+12V	- 1.5 A
+VCC3	- 9A
+3V3_S5 (wake)	- 1.125A
+3V3_S5 (no wake)	- 20mA



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M.2 1 Connector

M2下方零件擺放限高要小於0.9mm的零件

VCC3 4.25A  
Max: 14W

LANE REVERSE TO SUPPORT SATA SSD

2020.03.25

2020.03.25

2020.03.25

2020.04.07


2020.04.16

2020.03.25 SMBUS Level Shift IC

pull high ESIO SIDE

CPU Side pull high 4.7K

Footprint: H\_R240D173\_BR189\_PT



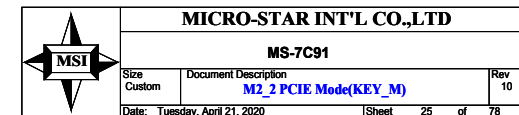
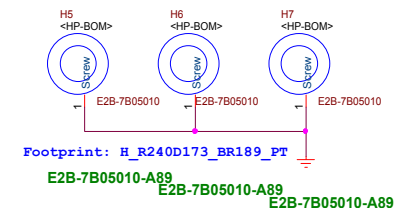
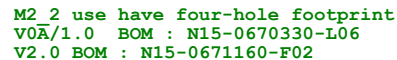
MICRO-STAR INT'L CO.,LTD

MS-7C91

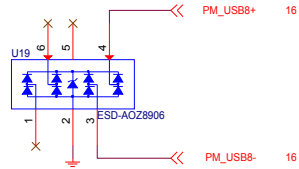
Size Custom Document Description M2\_1 PCIE/SATA Mode(KEY\_M) Rev 10

Date: Tuesday, April 21, 2020 Sheet 24 of 78

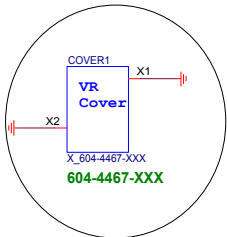
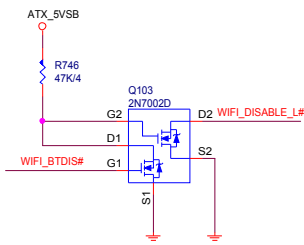
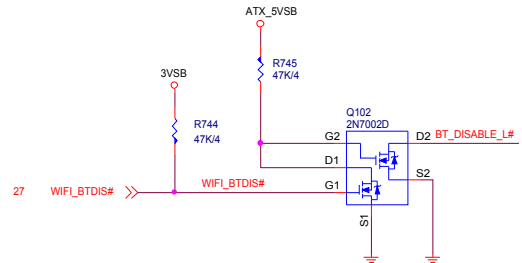
VCC3 4.25A  
Max: 14W



# EMI NEAR CONNECTOR



3VSB C867 X 0.1u16X

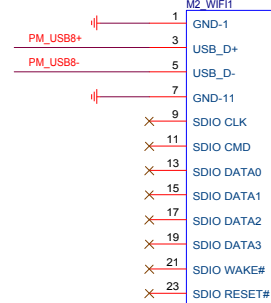


E43-1204046-P65

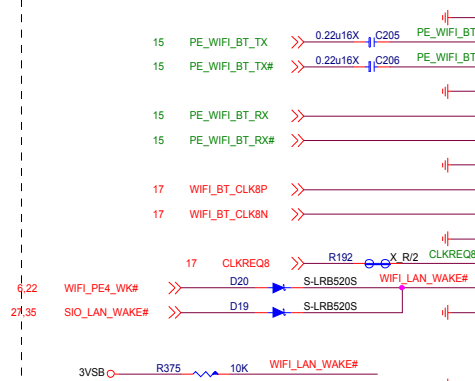
E43-1204046-P65



604-4467-020



KEY E



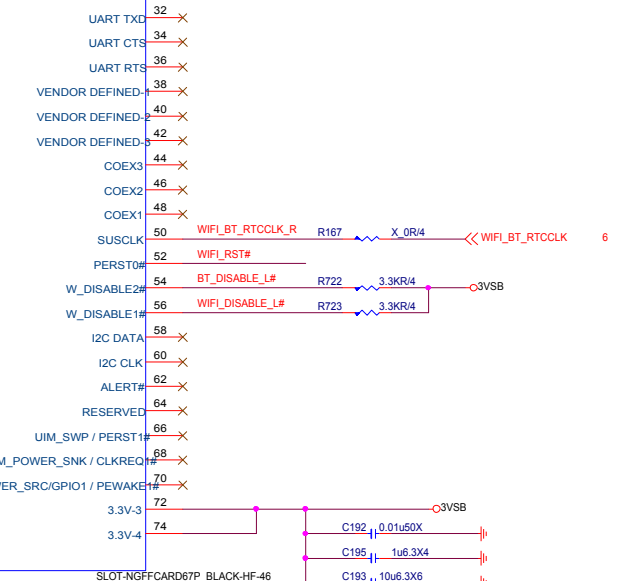
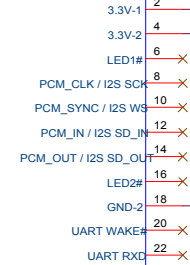
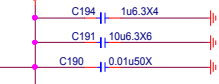
N15-0670610-L06

MEC2

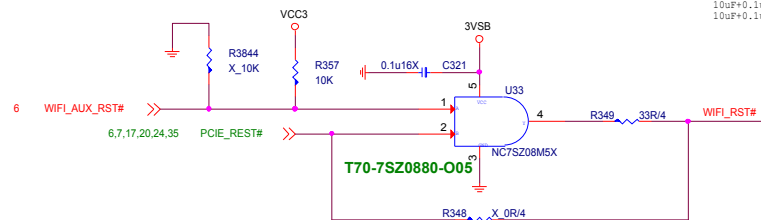
MEC1

780mA

3VSB



10uF\*0.1uF\*0.01uF at one end of socket in support of 3.3 V3V pins 2 and 4.  
10uF\*0.1uF\*0.01uF at the other end of the socket in support of 3.3 V3V pins 70 and 72.



T70-7SZ0880-O05



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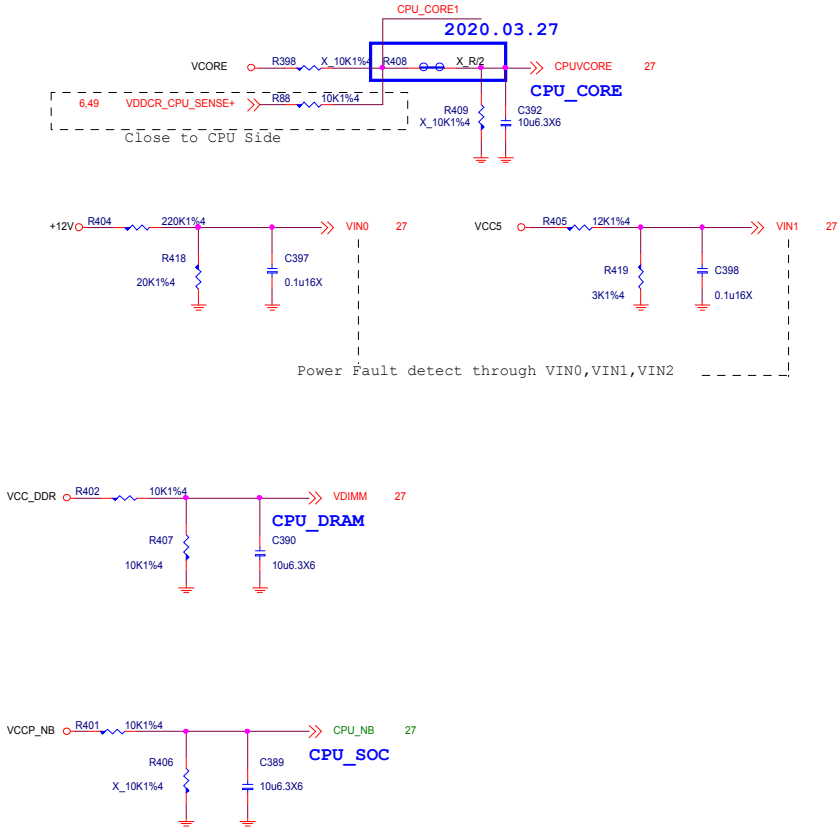
Size	Document Description	Rev
Custom	M2_2 - WIFI+BT	10
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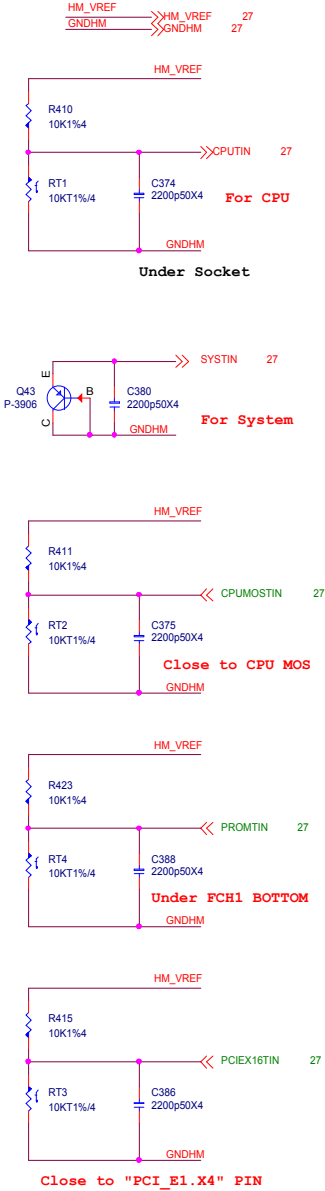
# HW Monitor - Voltage

SIO HM Voltage over 2.048V will not detect



Power Fault detect through VIN0,VIN1,VIN2

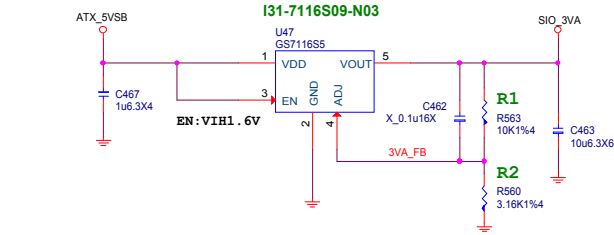
## TEMP SENSOR



## PM RESET

## CPU RESET

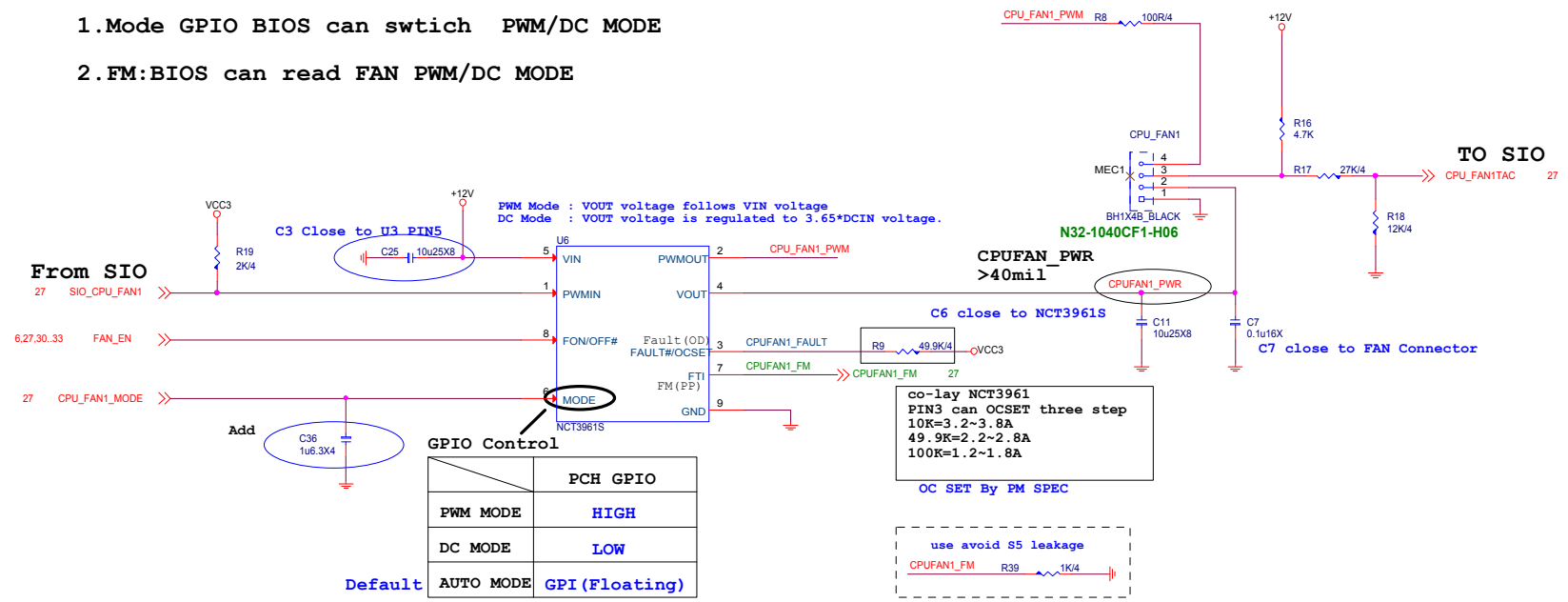
## SIO\_3VA



$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.8 * (1 + (10K/3.16K)) \\ &= 3.33V \end{aligned}$$

CPUFAN1 TYPE N : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

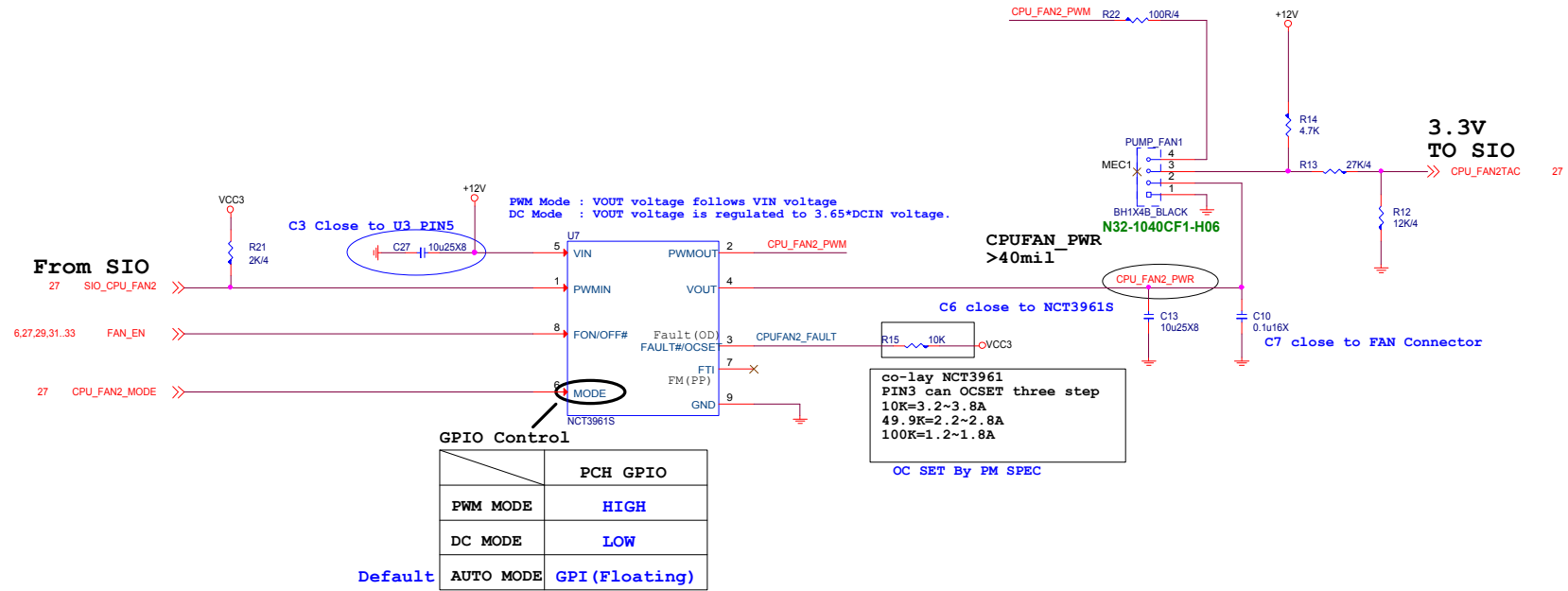
- 1.Mode GPIO BIOS can swtich PWM/DC MODE
- 2.FM:BIOS can read FAN PWM/DC MODE



# PUMPFAN1

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



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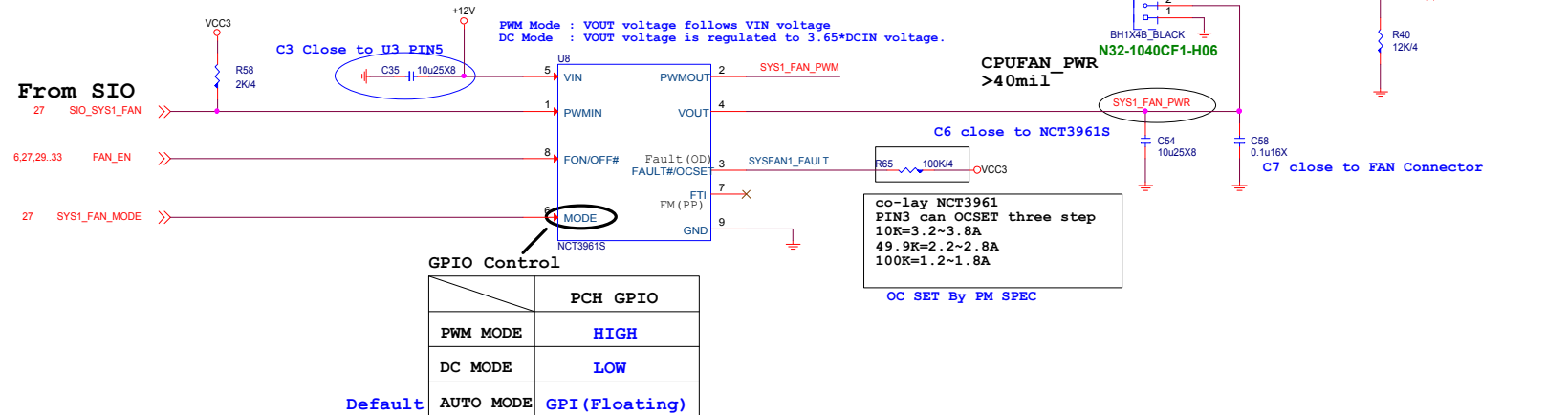
MS-7C91

Size Custom	Document Description FAN TYPE-K PUMPFANI	Rev 10
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## SYSFAN1

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

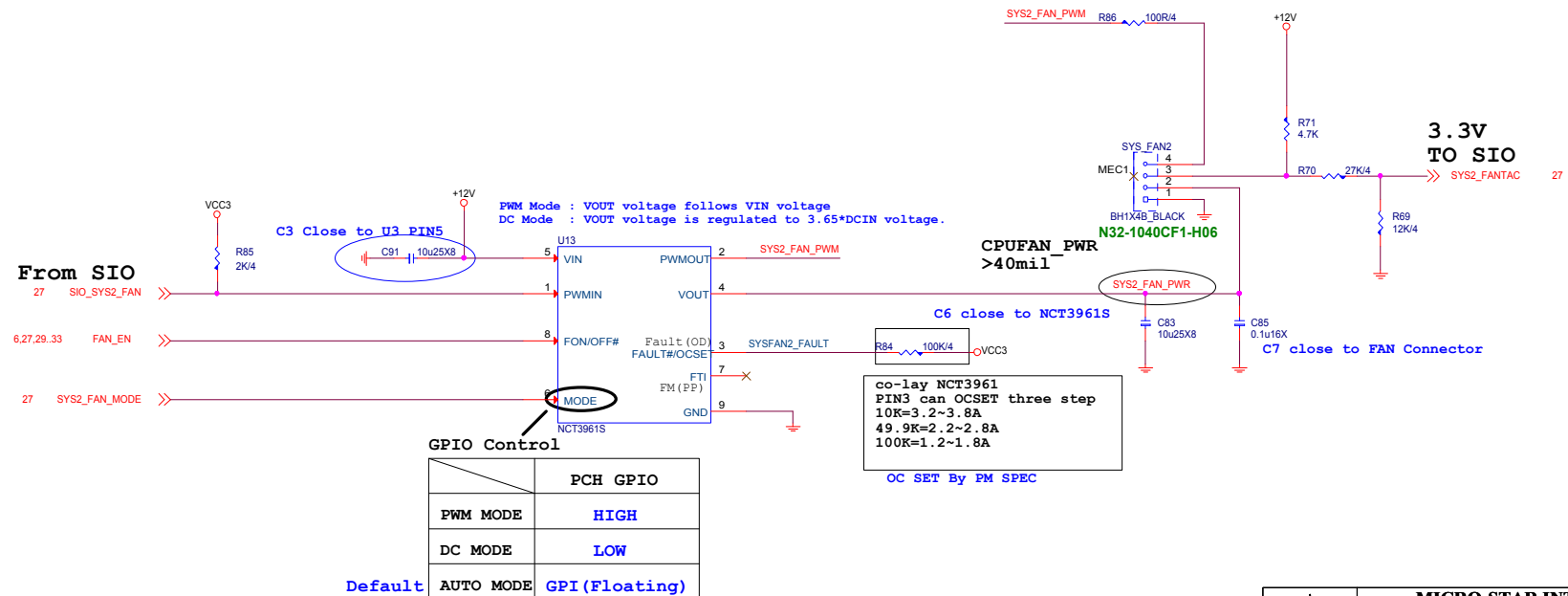
1.Mode GPIO BIOS can switch PWM/DC MODE



## SYSFAN2

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

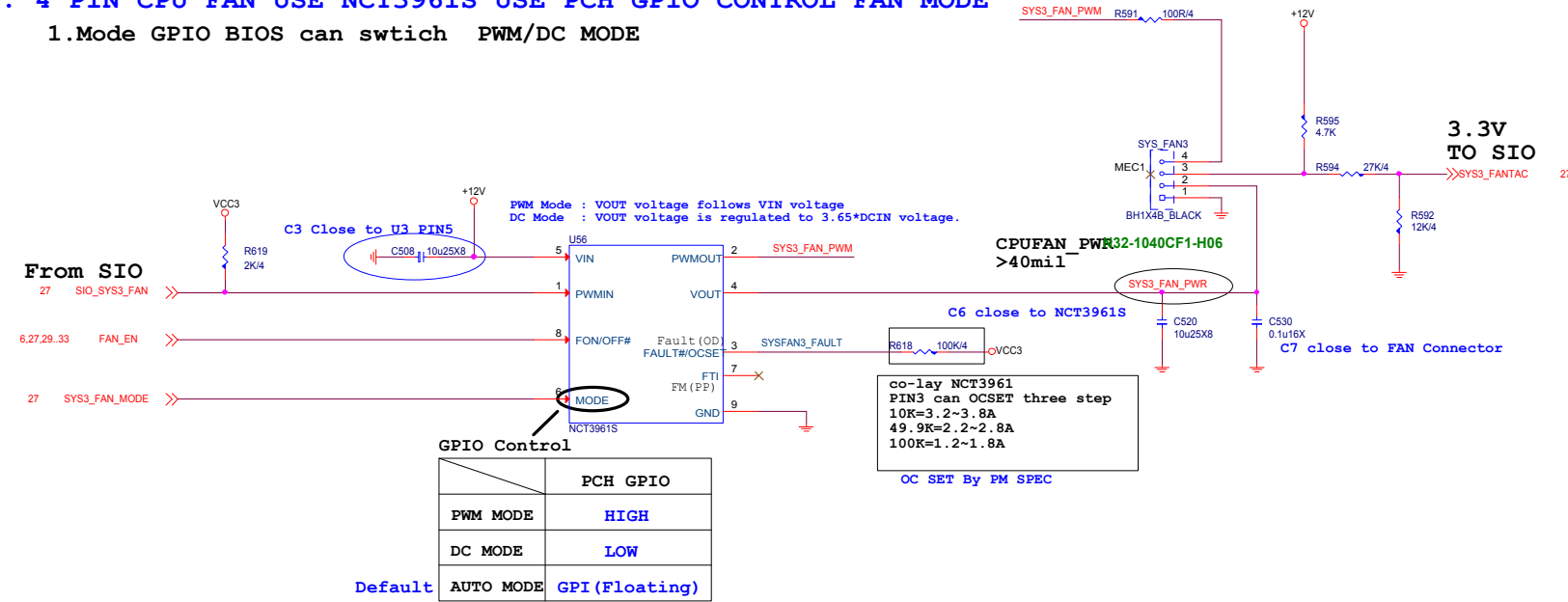
1.Mode GPIO BIOS can switch PWM/DC MODE



# SYSFAN3

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

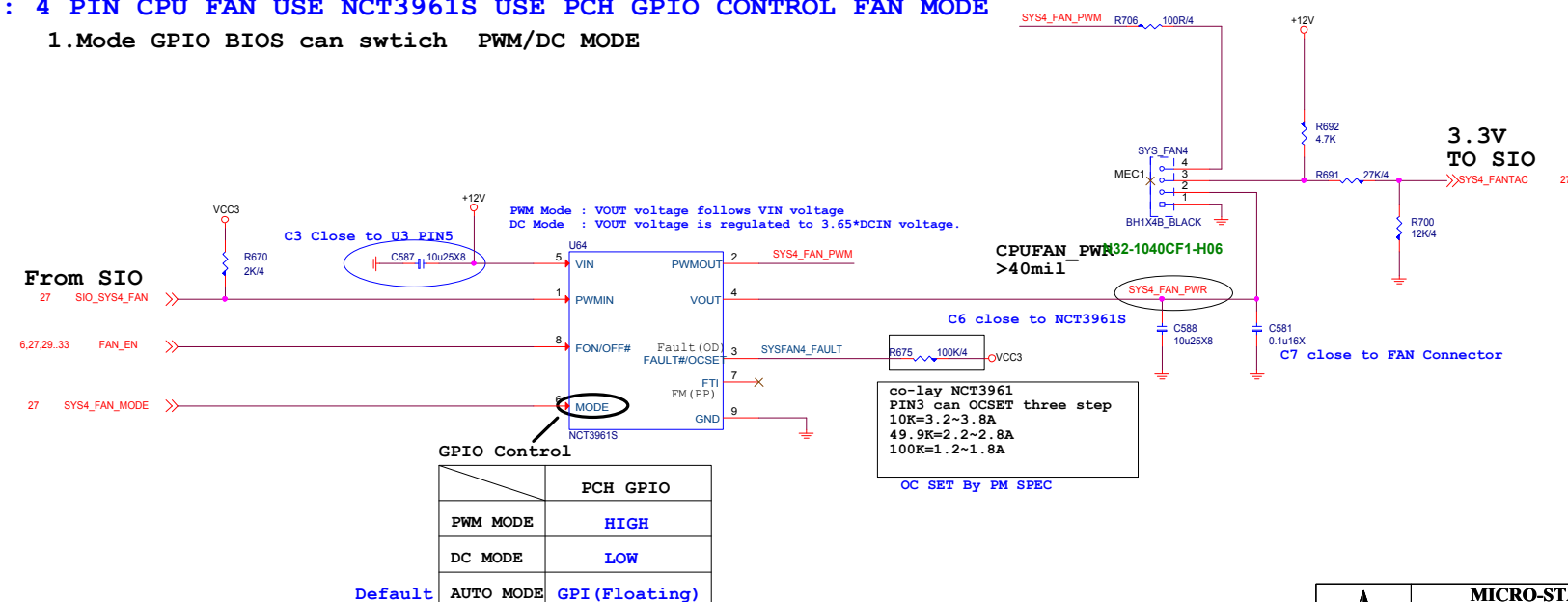
1.Mode GPIO BIOS can swtich PWM/DC MODE



# SYSFAN4

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

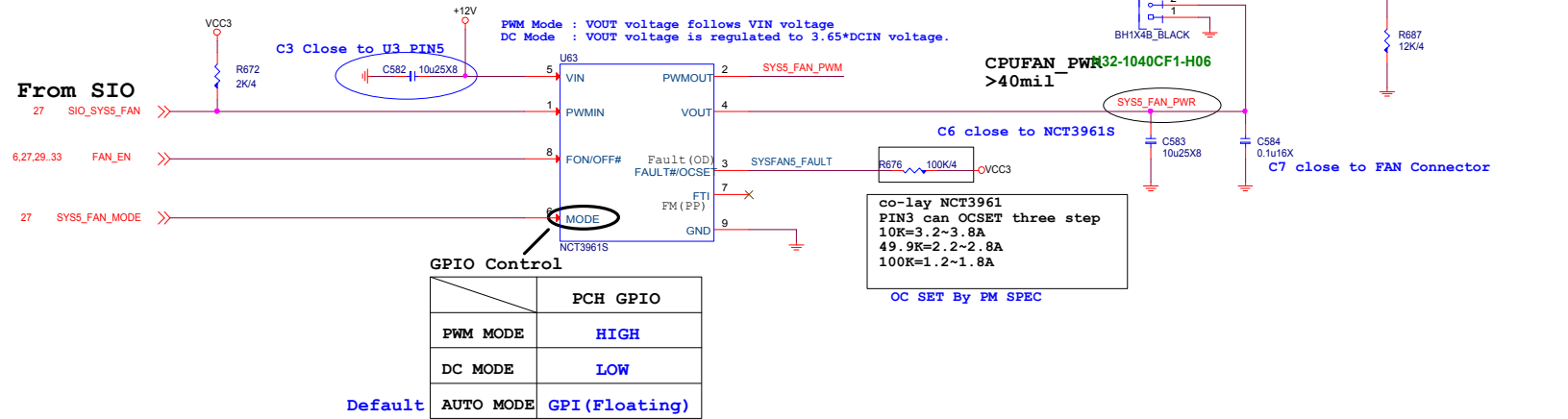
1.Mode GPIO BIOS can swtich PWM/DC MODE





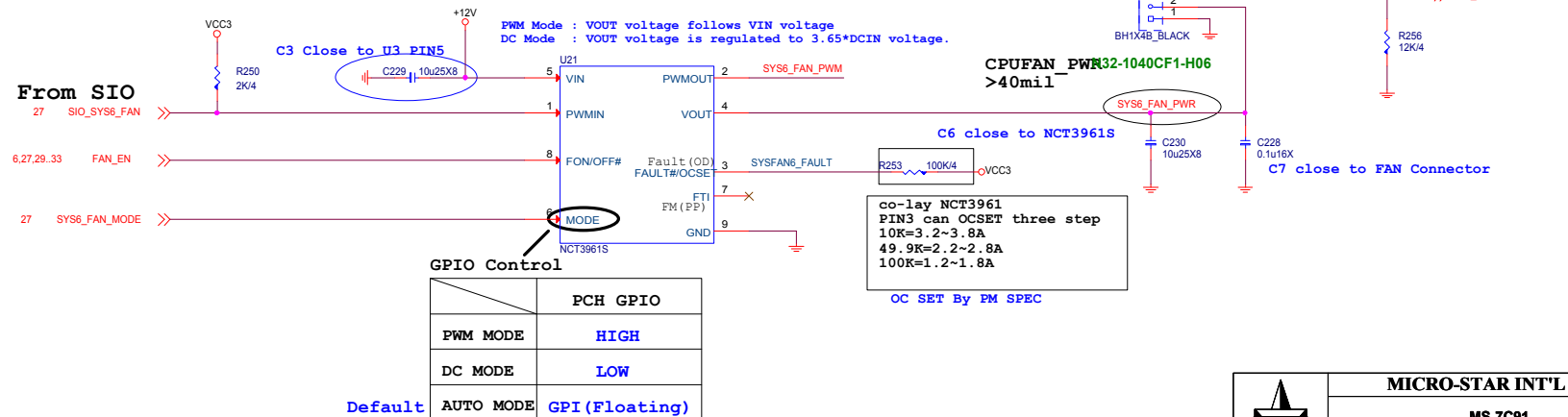
# **SYSFAN5 TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE**

1.Mode GPIO BIOS can swtich PWM/DC MODE



# **SYSFAN6 TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE**

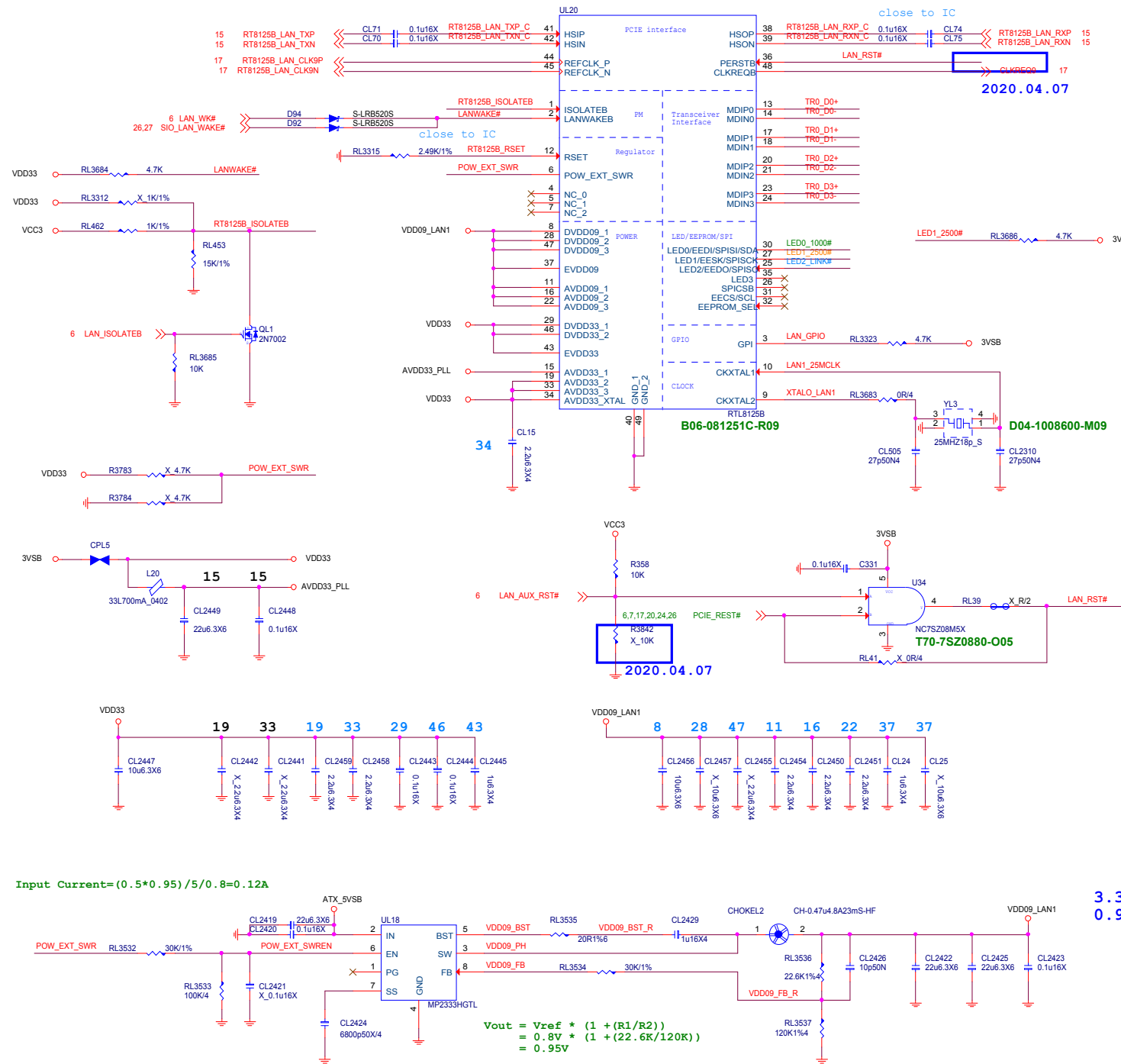
1.Mode GPIO BIOS can swtich PWM/DC MODE



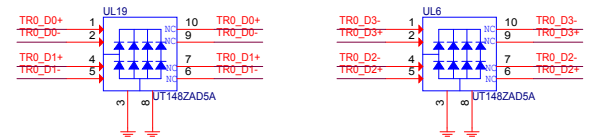
**RTL8111H Giga LAN**

2020.04.16

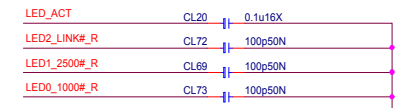
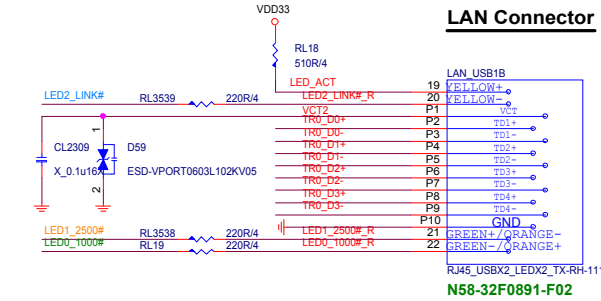
Realtek Lan1-RTL8125B(2.5G)



ESD Protect  
close to connector



LAN Connector



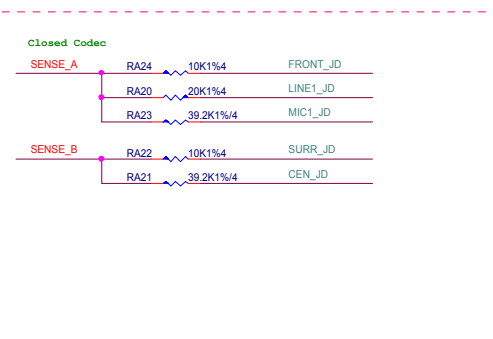
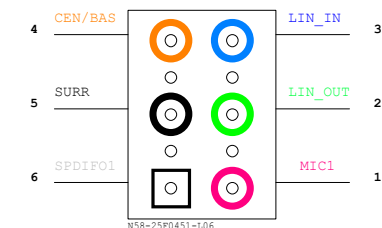
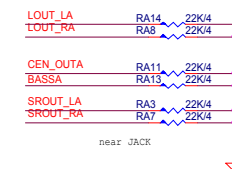
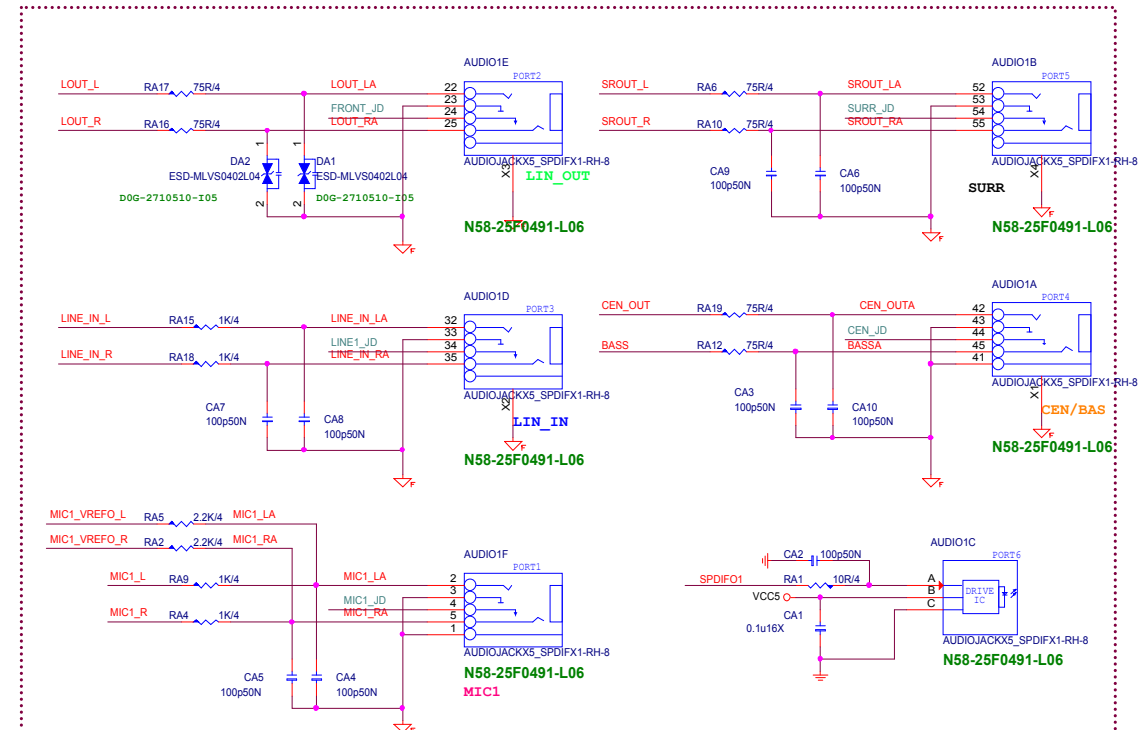
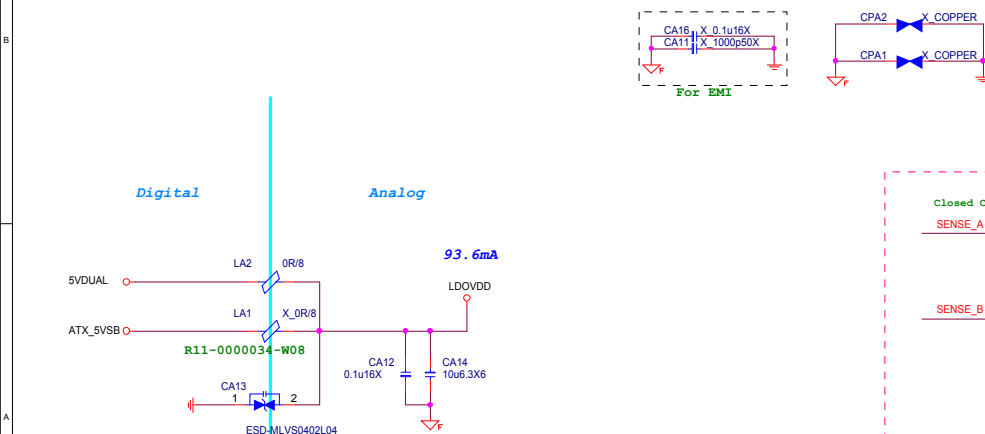
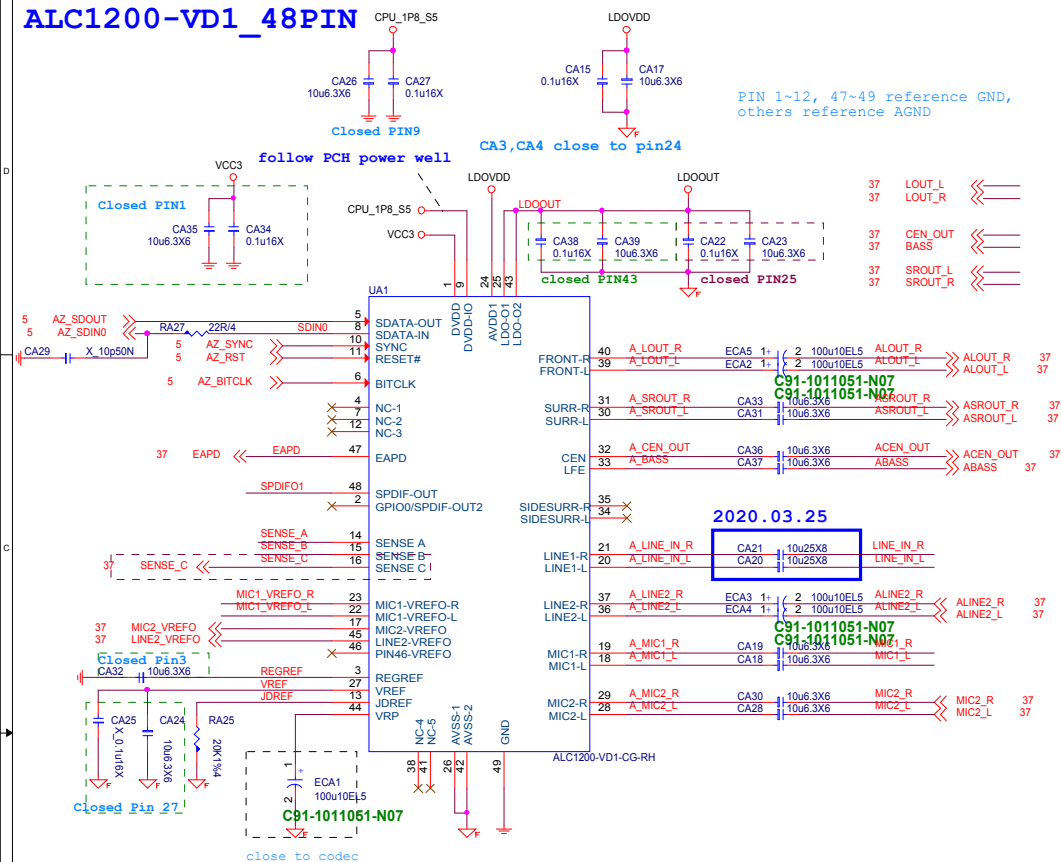
2020.04.07  
Removed

Input Current=(0.5\*0.95)/5/0.8=0.12A

3.3V Icc Max:100mA  
0.95V Icc Max:650mA

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# ALC1200-VD1 48PIN

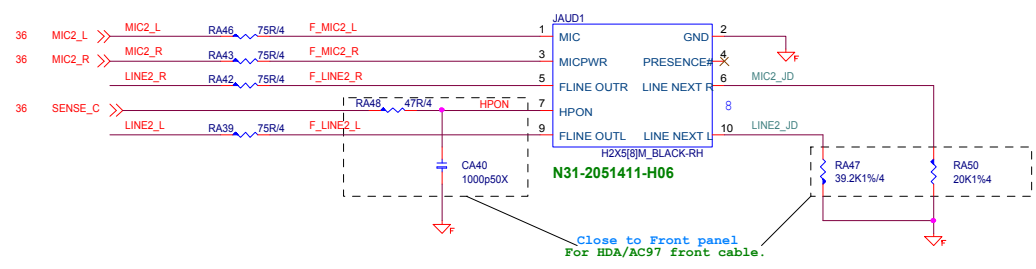
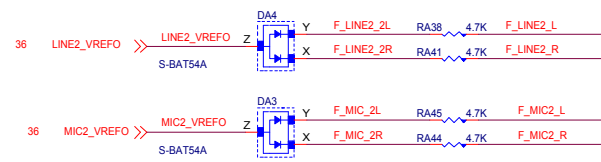


**MICRO-STAR INT'L CO.,LTD**

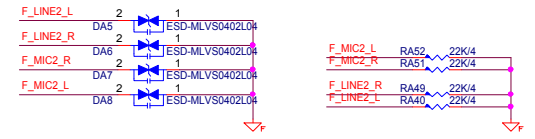
MS-7C91

Size Custom	Document Description <b>Audio ALC1200-VD1</b>
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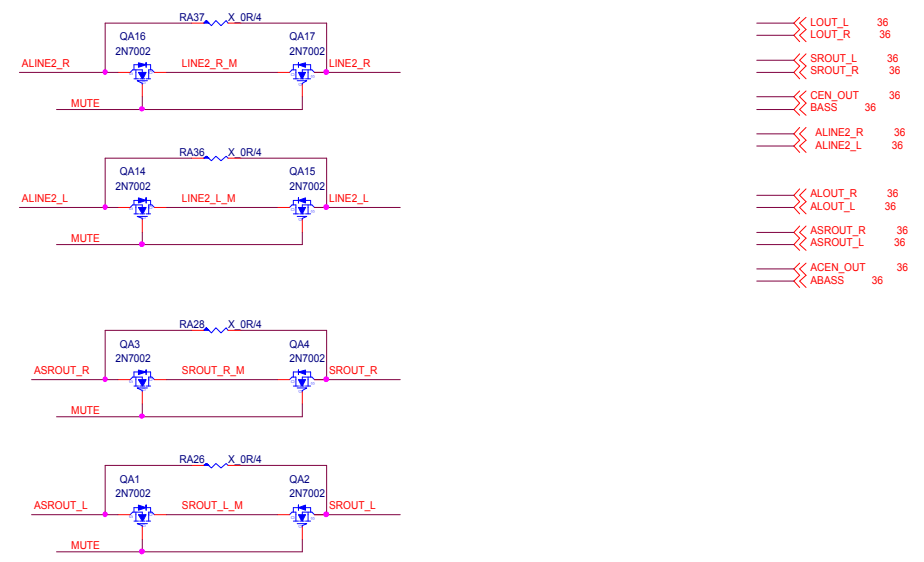
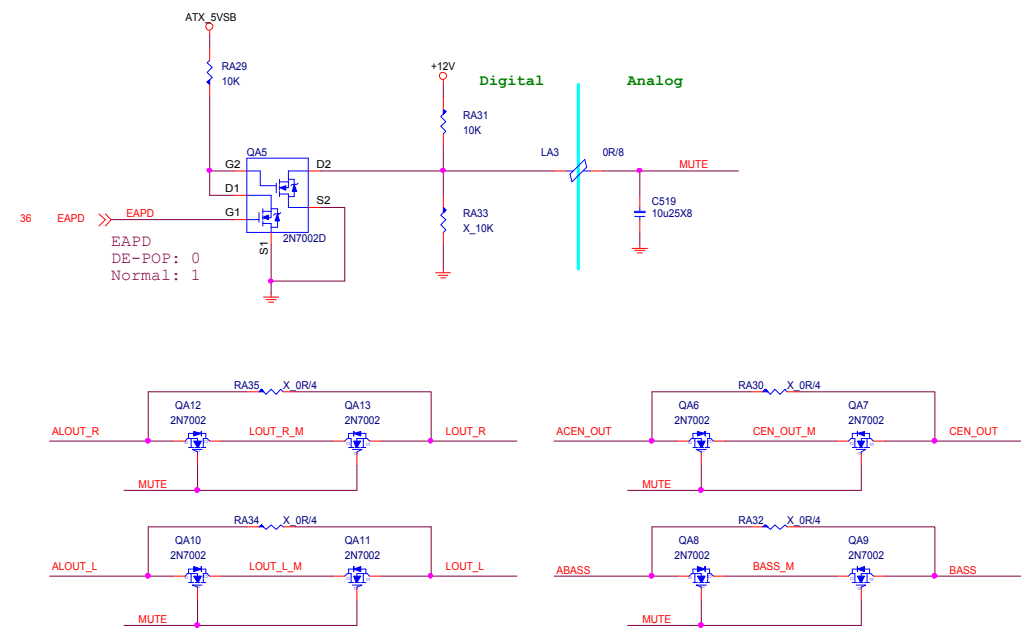
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D0G-2710510-I05  
Close to Front panel  
**ESD protect**  
D0G-2710510-I05  
AVL:D0G-2950500-S10



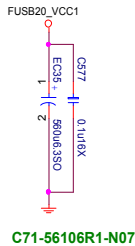
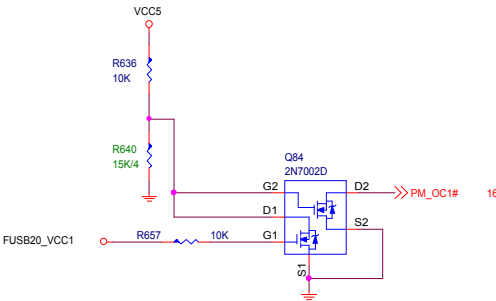
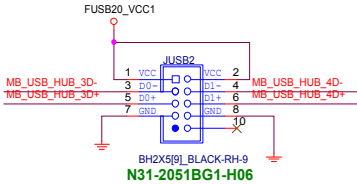
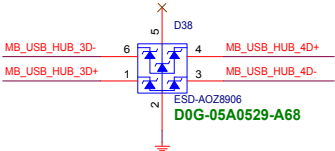
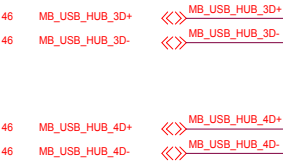
De-POP circuit



[illegible]

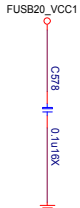
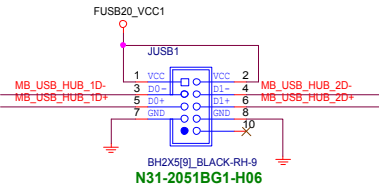
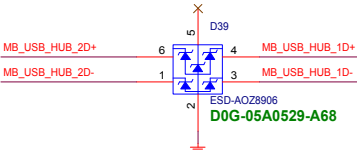
Front USB2.0 (JUSB2) Form GL850G USB2.0 HUB

5V@1A

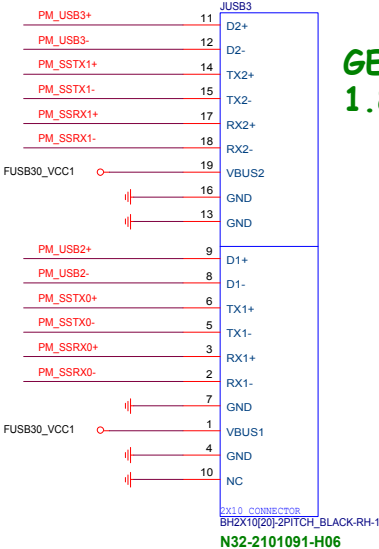
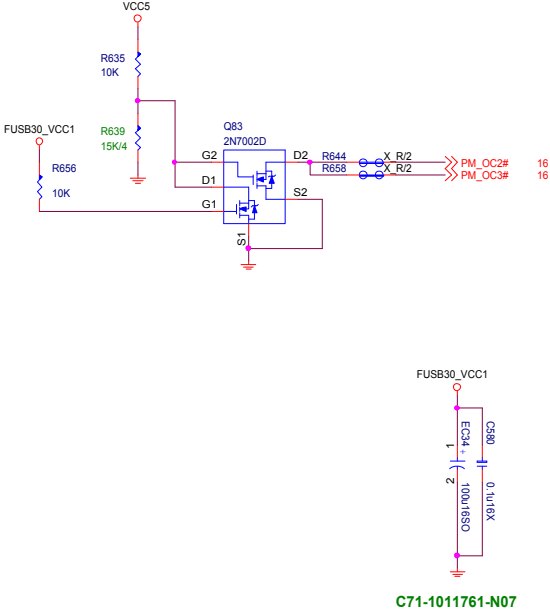
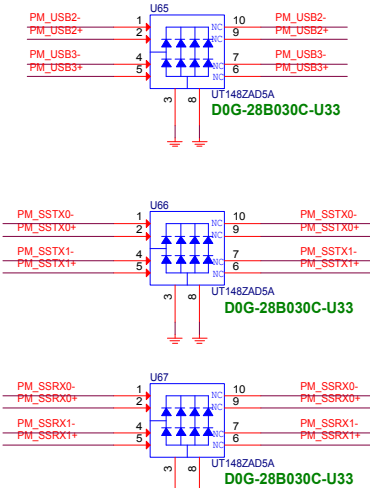
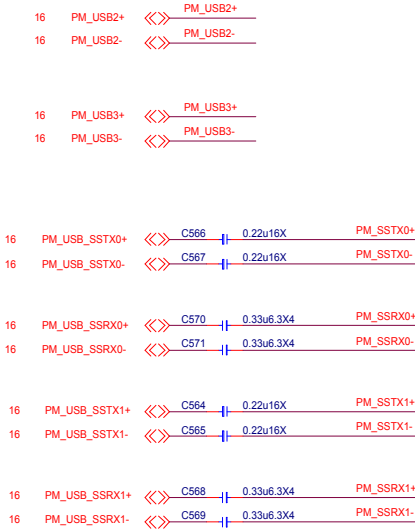


Front USB2.0 (JUSB1) Form GL850G USB2.0 HUB

5V@1A

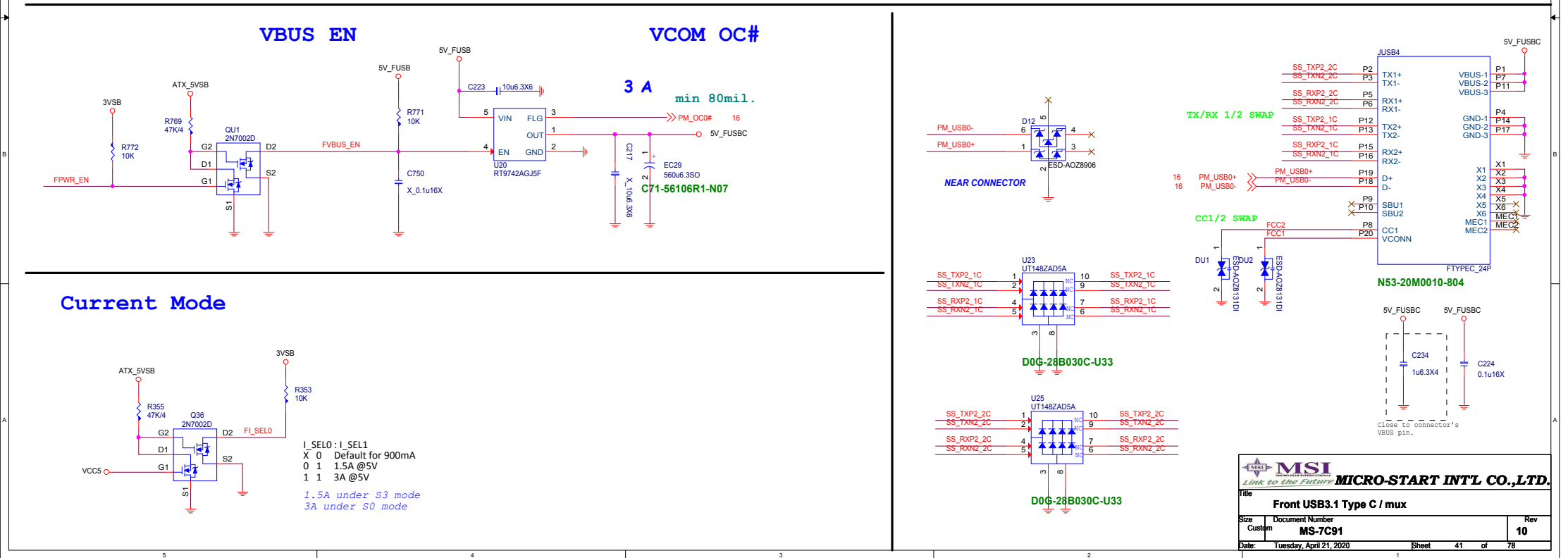
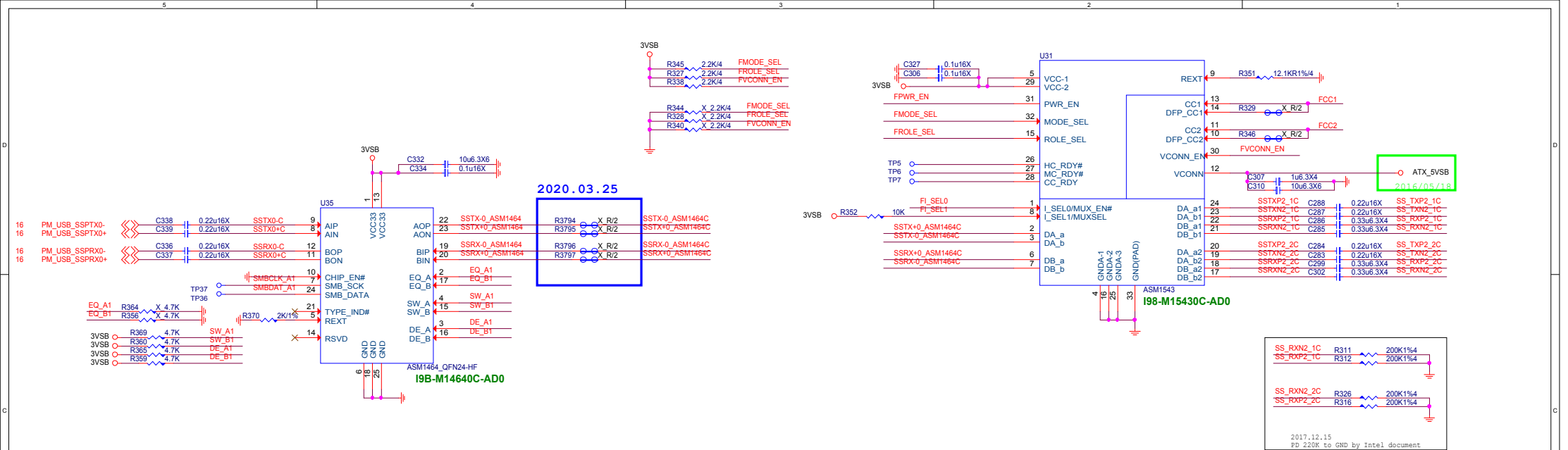


Front USB3 180°  
BOX Header(JUSB3)  
5V@1.8A

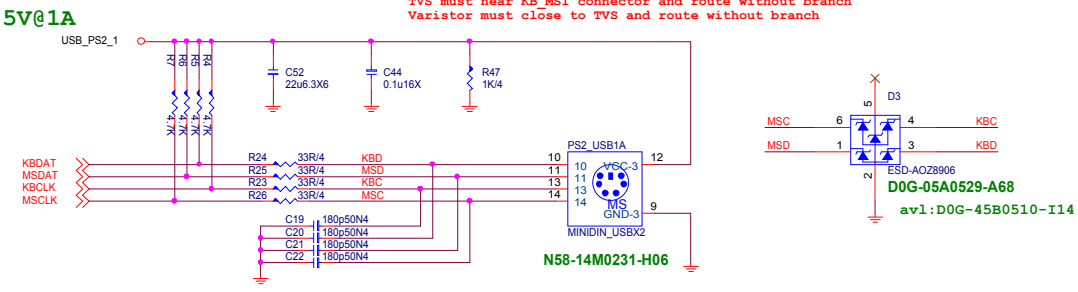


GEN1  
1.8A





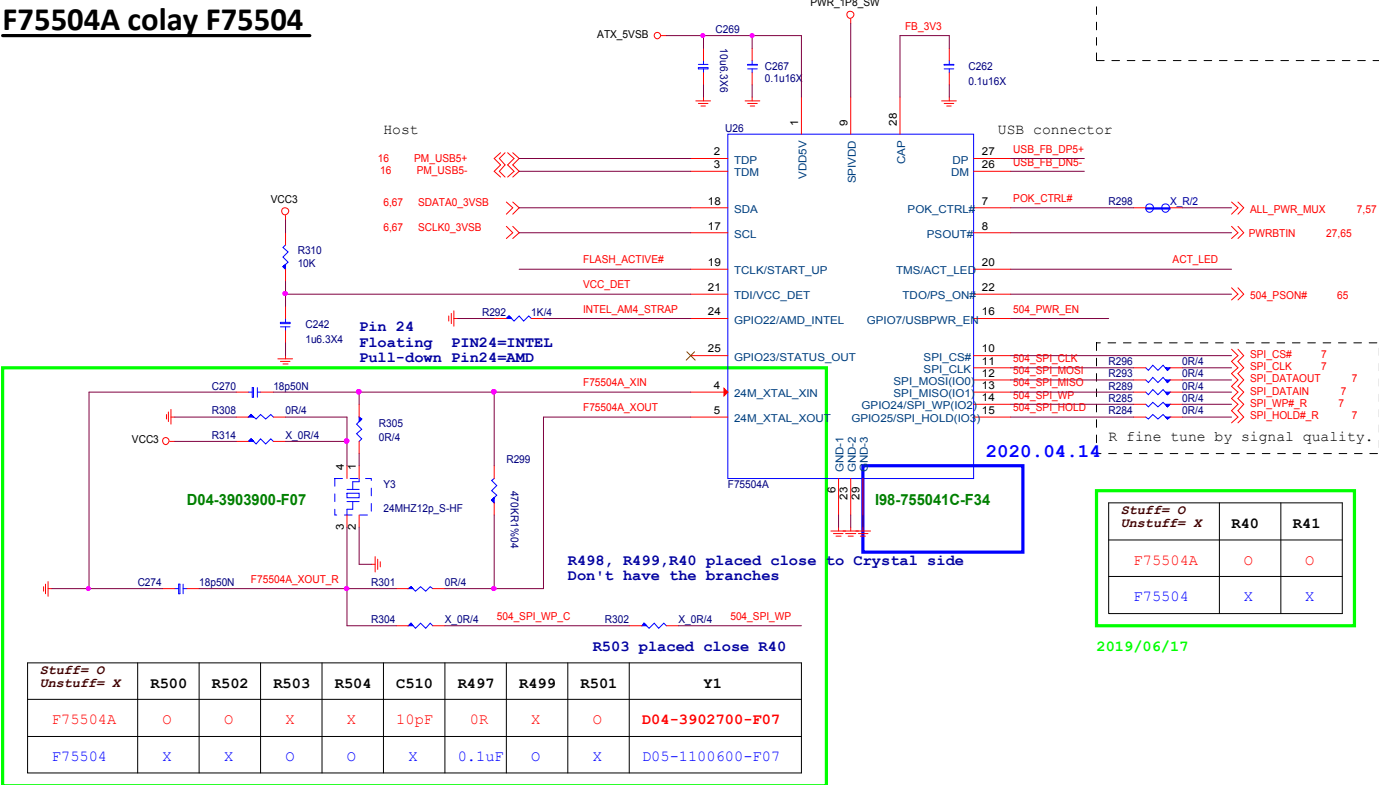
PS2+USB (USB2.0)



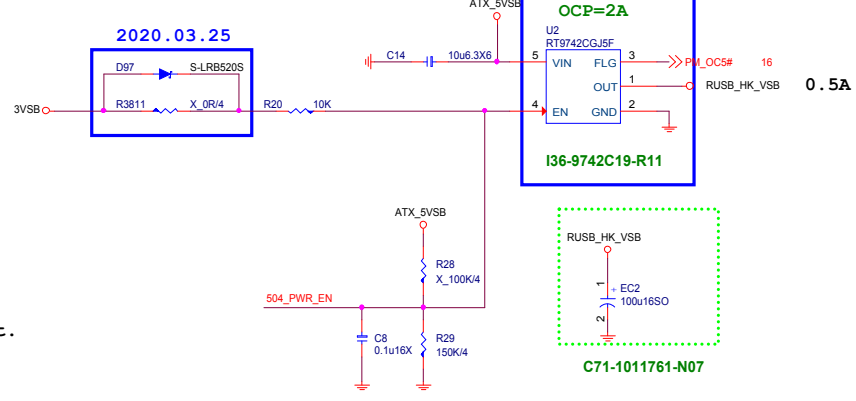
USB Flash BIOS

F75504A colay F75504

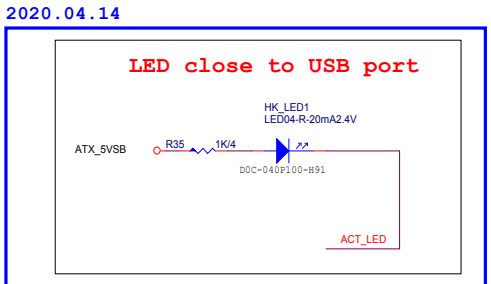
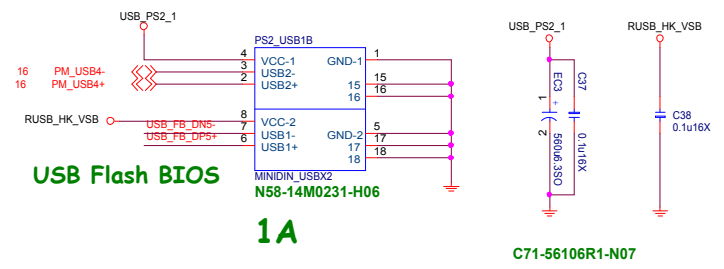
F75504A/F75504 layout placement must meet to spi/usb trace length spec with host.  
As for as possible place near to host.



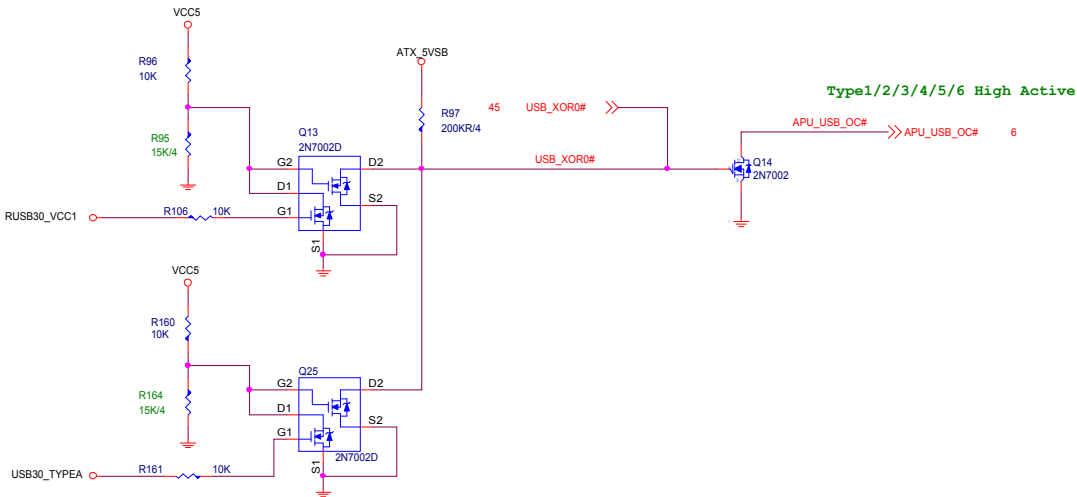
HOTKEY POWER



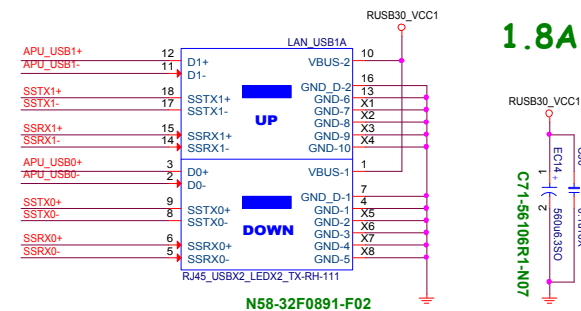
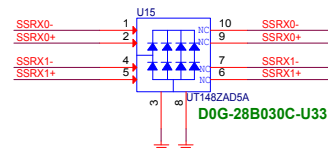
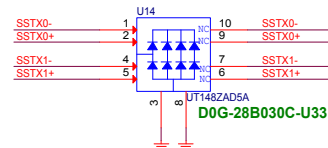
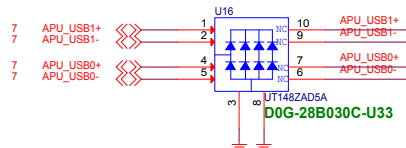
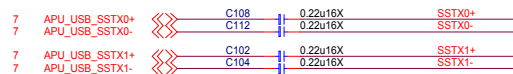
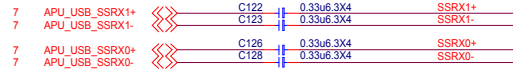
USB Flash BIOS



## CPU USB\_OC



## Rear USB3.1 GEN1 5V@1.8A



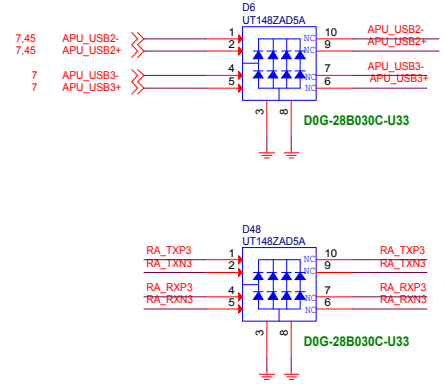
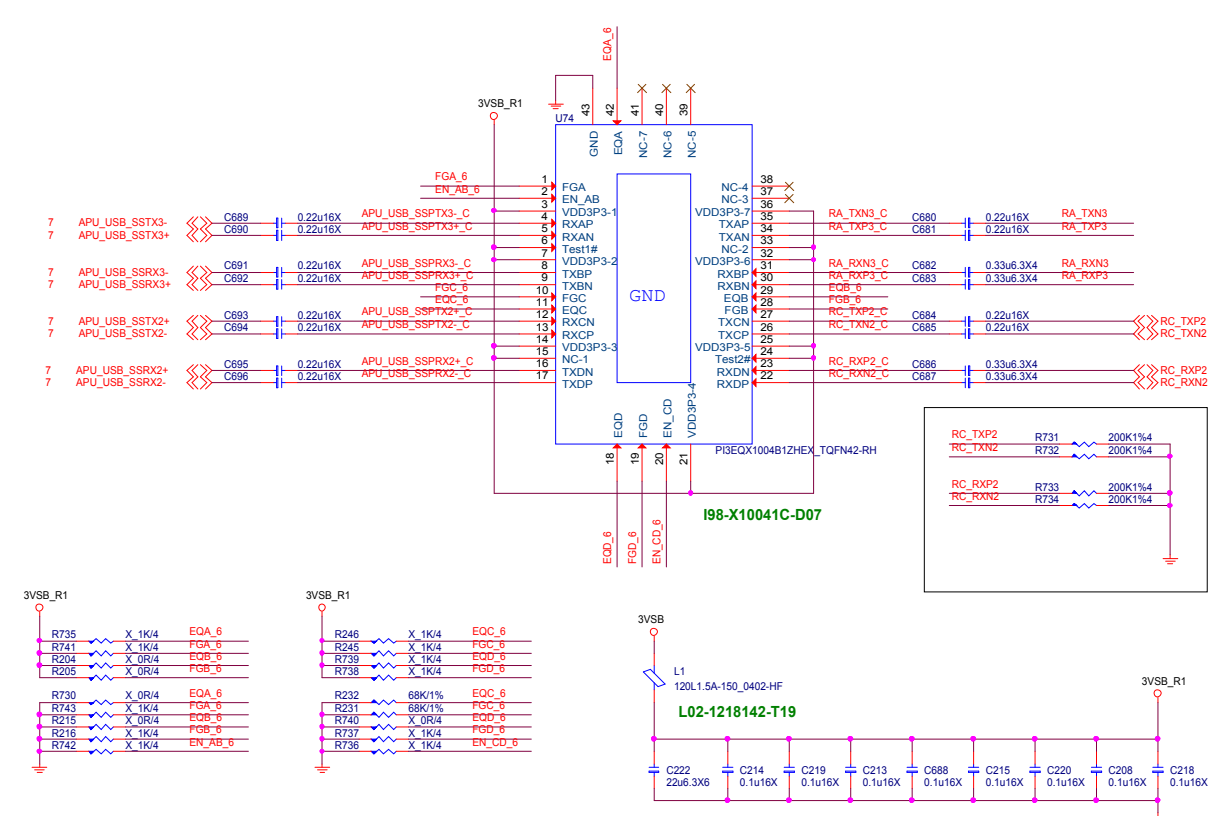
**MICRO-STAR INT'L CO.,LTD**

MS-7C91

Size Custom	Document Description <b>Rear USB3.1.</b>
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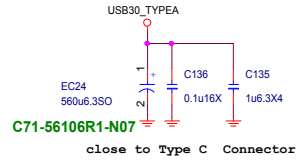
Rev	10
78	

## TYPE-A PI3EQX1004 Redriver



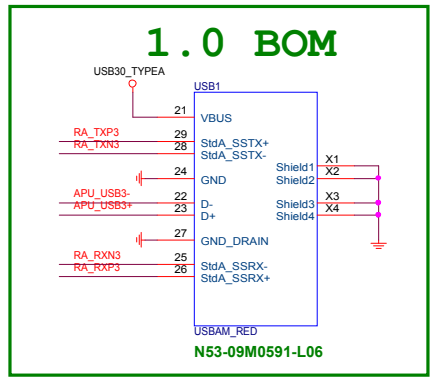
| Rear TYPE-A

Rear TYPE-C



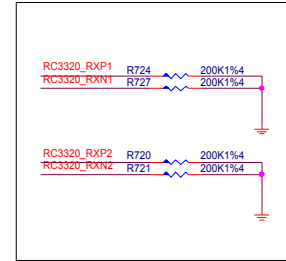
GEN2 0.9A

2020.04.16

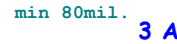


EQ	dB				EQ	FG		FG	dB	
0	10.9	0 to GND		USB3_TX4	A	R	F	0	-3	0 to GND
R	6.7	68K to GND		USB3_RX4	C	R	L	R	-1.5	68K to GND
F	8.9	NC		USB3_TX3	B	R	F	F	0	NC
1	13.1	0 to VDD		USB3_RX3	D	R	L	1	2	0 to VDD

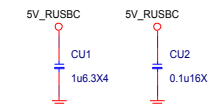
## USB Type-C MUX with Configuration Channel (CC)



## VBUS EN



Current Mode



MS-7C91

**Rear USB3.1 Type C / mux**

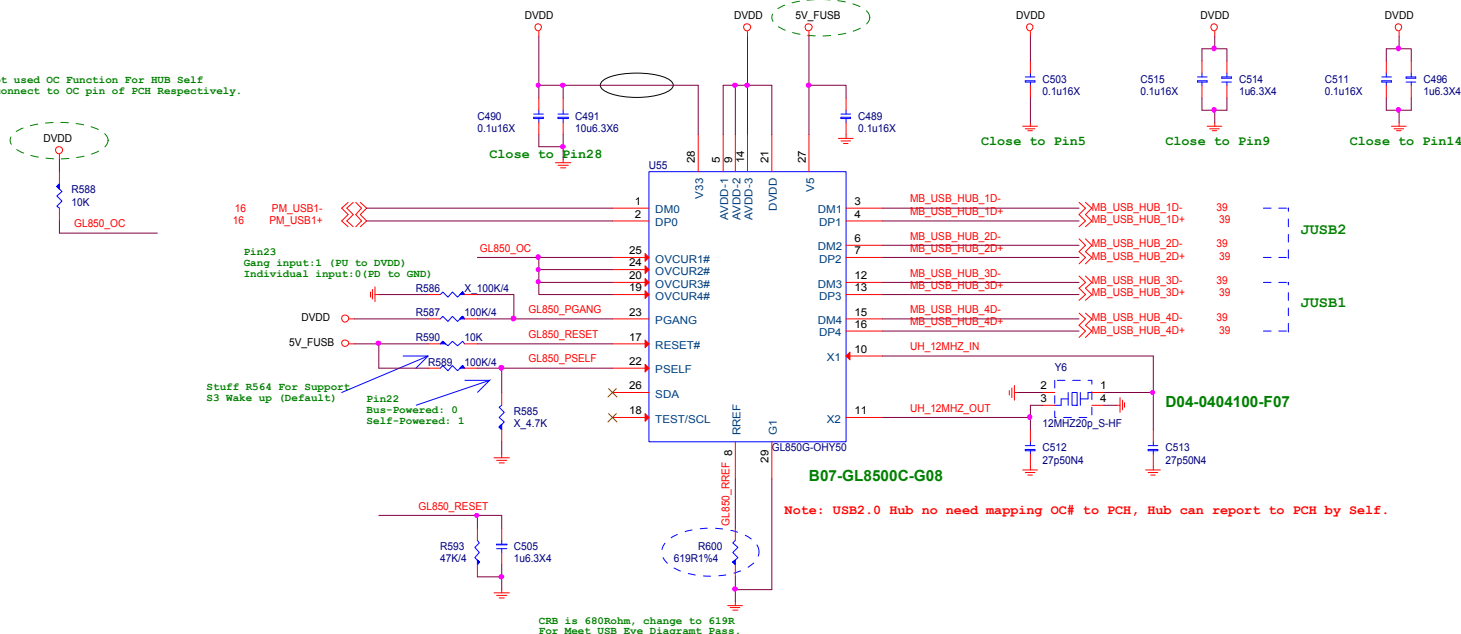
Size Custom	Document Description <b>Rear USB3.1 Type C / mux</b>	Rev 10
Date: Tuesday, April 21, 2020		Sheet 45 of 78

# GL850G USB2.0 HUB

## 5V\_FUSB

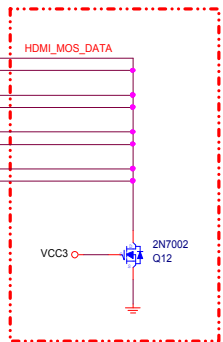
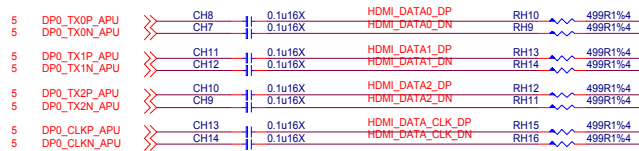
Note: Not used OC Function For HUB Self  
Please connect to OC pin of PCH Respectively.

Note: Please connect to USB Power Source.

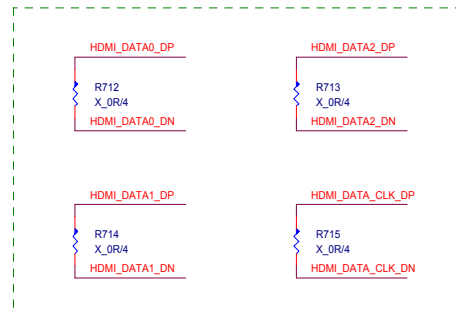


# HDMI CONNECTOR

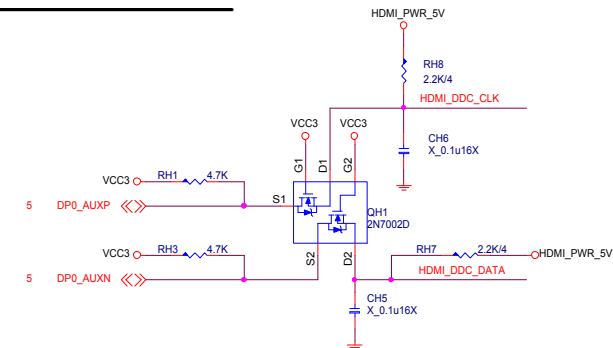
For HDMI 1.4



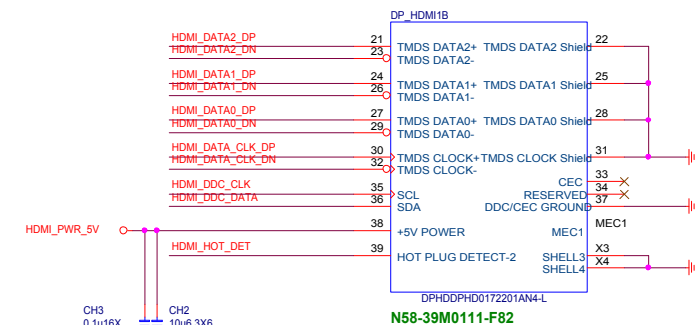
HDMI\_MOS\_DATA trace length <500mil  
other platform please check design guide



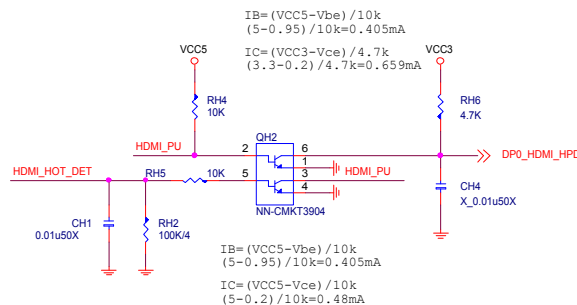
## AUX Level Shifter



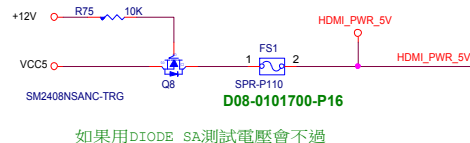
## Connector



## HPD Circuit

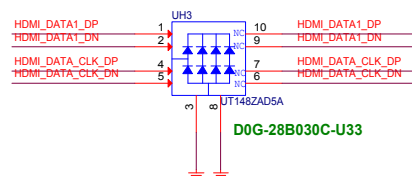
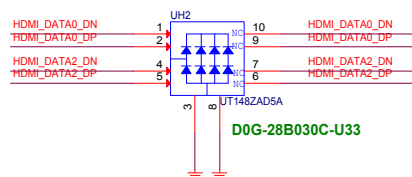


## Connector Power

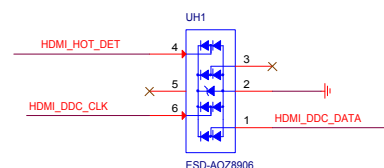


如果用DIODE SA測試電壓會不過

## For EMI

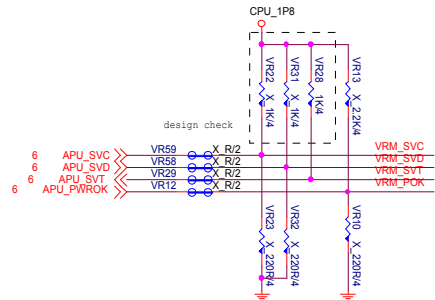


注意:耐壓5v零件



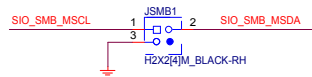




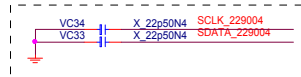


Note:VID Override Circuit

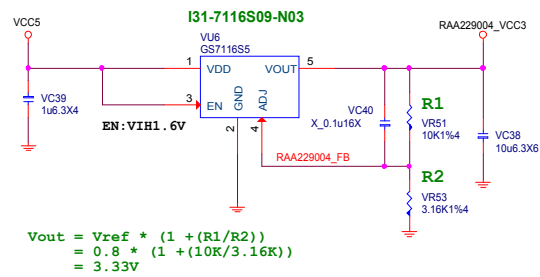
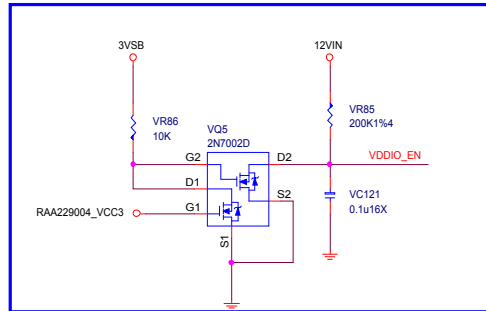
SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



SMBUS address:0X60(7 bit)  
0XC0(8 bit)



2020.04.09



$$V_{out} = V_{ref} * (1 + (R1/R2))$$

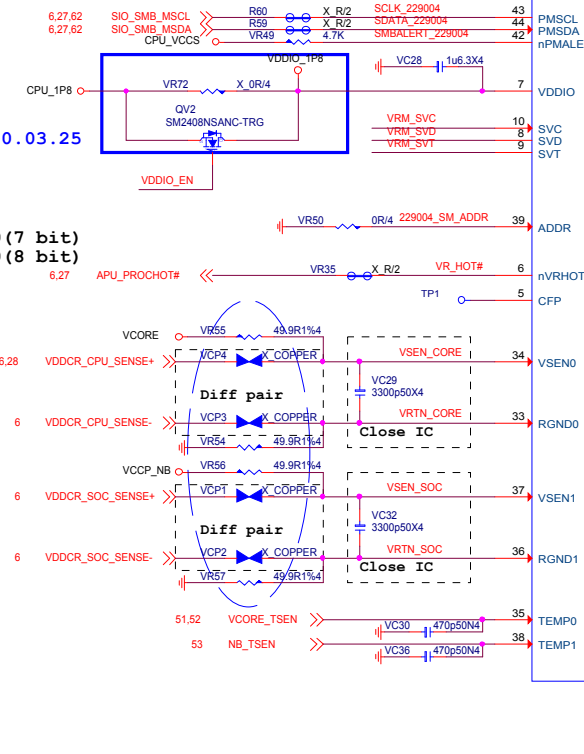
$$= 0.8 * (1 + (10K/3.16K))$$

$$= 3.33V$$

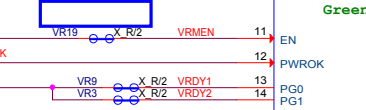


2020.03.25

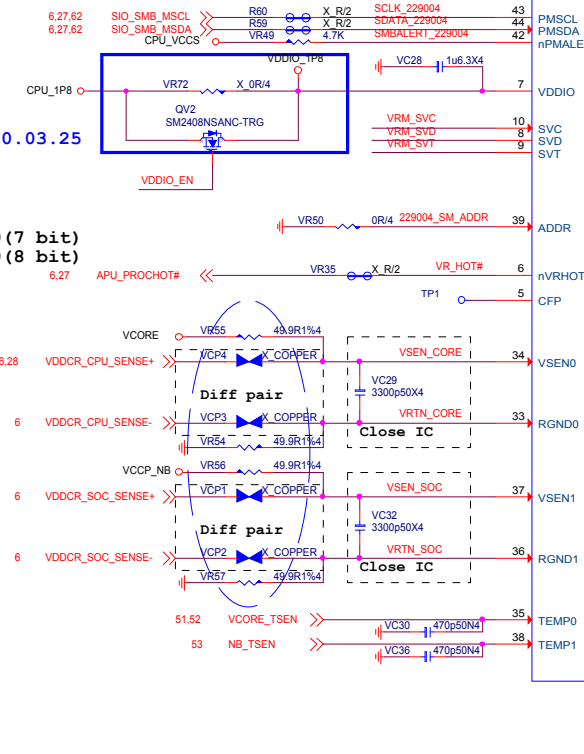
Condition as TSEN point



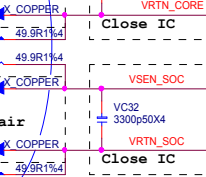
2020.03.25



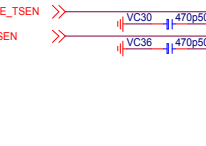
Condition as TSEN point



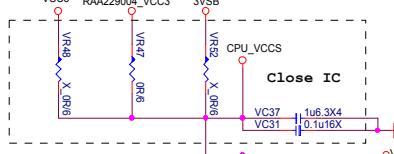
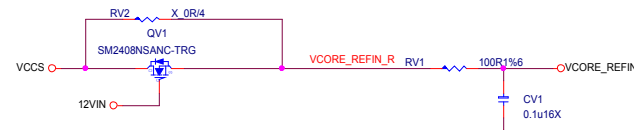
Diff pair



Diff pair



PWM SIDE



VCC3

RAA229004\_VCC3

3VSB

CPU\_VCCS

Close IC

VC37 1u6.3X4

VC31 0.1u16X

VC35 4.7u6.3X6

VC33 1000p50X

VC27 1000p50X

VC26 1000p50X

VC23 1000p50X

VC22 1000p50X

VC19 1000p50X

VC28 1u6.3X4

VC21 470p50N4

VC20 470p50N4

VC30 470p50N4

VC36 470p50N4

VC33 1000p50X

VC27 1000p50X

VC26 1000p50X

VC23 1000p50X

VC22 1000p50X

VC19 1000p50X

VC28 1u6.3X4

VC21 470p50N4

VC20 470p50N4

VC30 470p50N4

VC36 470p50N4

VC33 1000p50X

VC27 1000p50X

VC26 1000p50X

VC23 1000p50X

VC22 1000p50X

VC19 1000p50X

VC28 1u6.3X4

VC21 470p50N4

VC20 470p50N4

VC30 470p50N4

VC36 470p50N4

VC33 1000p50X

VC27 1000p50X

VC26 1000p50X

VC23 1000p50X

VC22 1000p50X

VC19 1000p50X

VC28 1u6.3X4

VC21 470p50N4

VC20 470p50N4

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VC36 470p50N4

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VC22 1000p50X

VC19 1000p50X

VC28 1u6.3X4

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VC20 470p50N4

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VC33 1000p50X

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VC26 1000p50X

VC23 1000p50X

VC22 1000p50X

VC19 1000p50X

VC28 1u6.3X4

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VC20 470p50N4

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VC33 1000p50X

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VC26 1000p50X

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VC19 1000p50X

VC28 1u6.3X4

VC21 470p50N4

VC20 470p50N4

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VC23 1000p50X

VC22 1000p50X

VC19 1000p50X

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VC20 470p50N4

VC30 470p50N4

VC36 470p50N4

VC33 1000p50X

VC27 1000p50X

VC26 1000p50X

VC23 1000p50X

VC22 1000p50X

VC19 1000p50X

VC28 1u6.3X4

VC21 470p50N4

VC20 470p50N4

VC30 470p50N4

VC36 470p50N4

VC33 1000p50X

VC27 1000p50X

VC26 1000p50X

VC23 1000p50X

VC22 1000p50X

VC19 1000p50X

VC28 1u6.3X4

VC21 470p50N4

VC20 470p50N4

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VC36 470p50N4

VC33 1000p50X

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VC19 1000p50X

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VC22 1000p50X

VC19 1000p50X

VC28 1u6.3X4

VC21 470p50N4

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VC36 470p50N4

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VC27 1000p50X

VC26 1000p50X

VC23 1000p50X

VC22 1000p50X

VC19 1000p50X

VC28 1u6.3X4

VC21 470p50N4

VC20 470p50N4

VC30 470p50N4

VC36 470p50N4

VC33 1000p50X

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VC26 1000p50X

VC23 1000p50X

VC22 1000p50X

VC19 1000p50X

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VC33 1000p50X

VC27 1000p50X

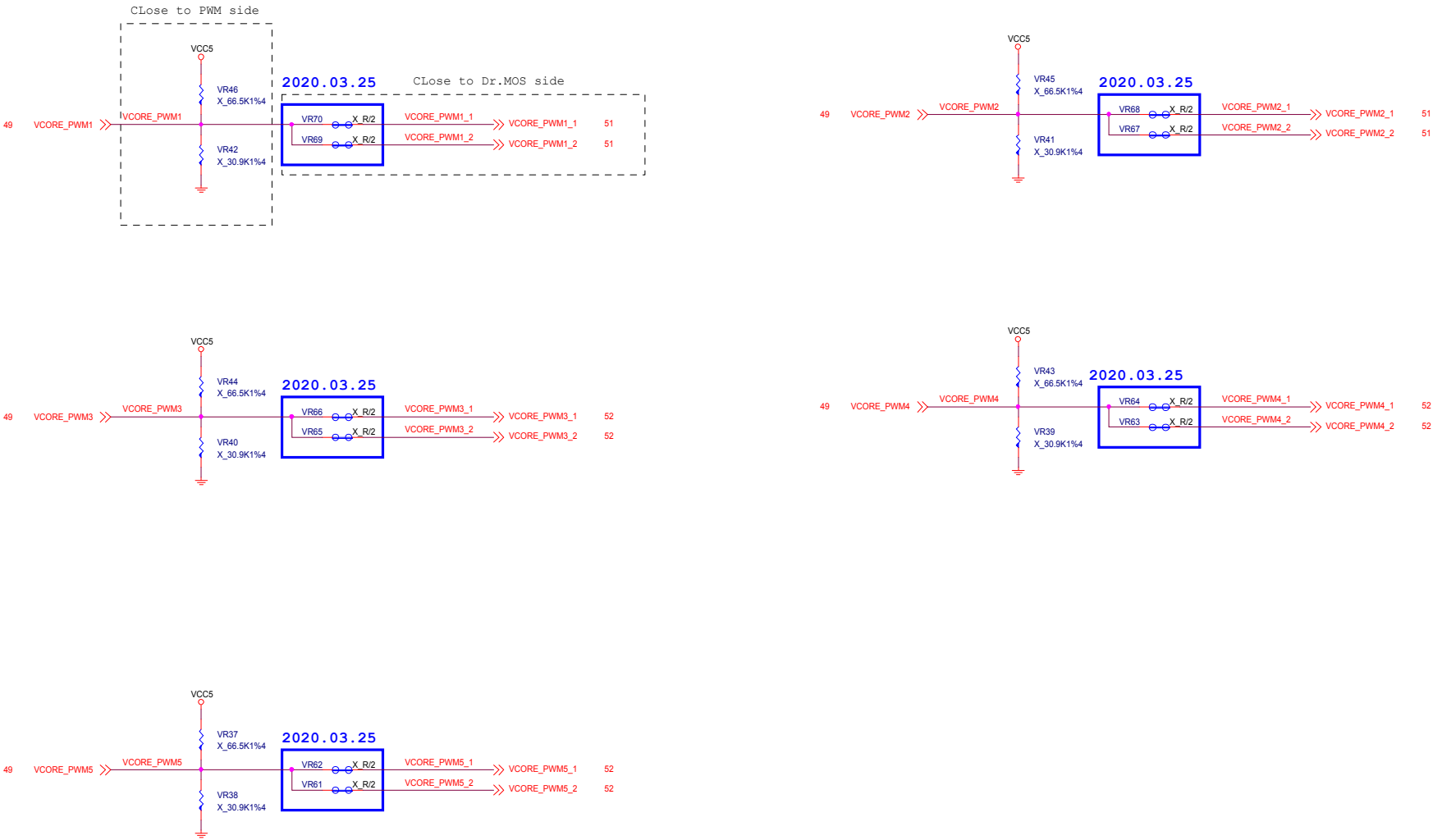
VC26 1000p50X

VC23 1000p50X

VC22 1000

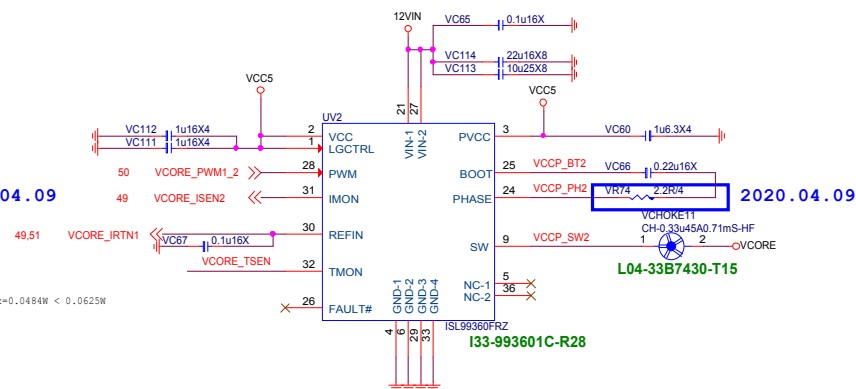
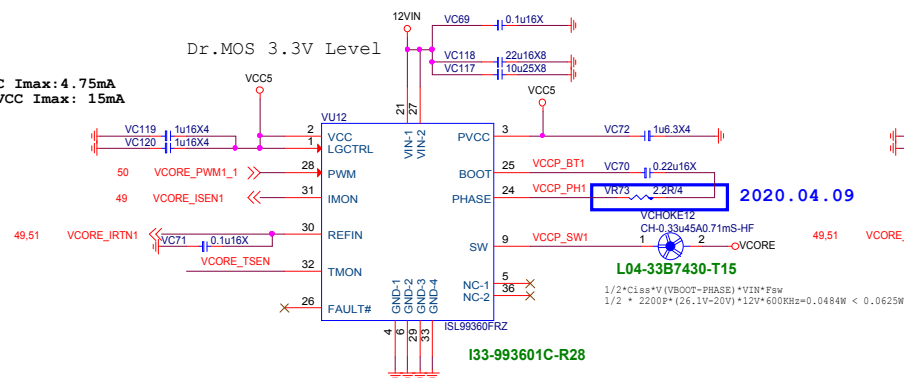
CPU\_CORE Driver IC

VCORE Double 10-PHASE

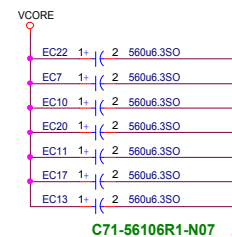
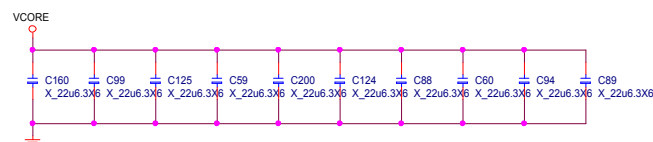
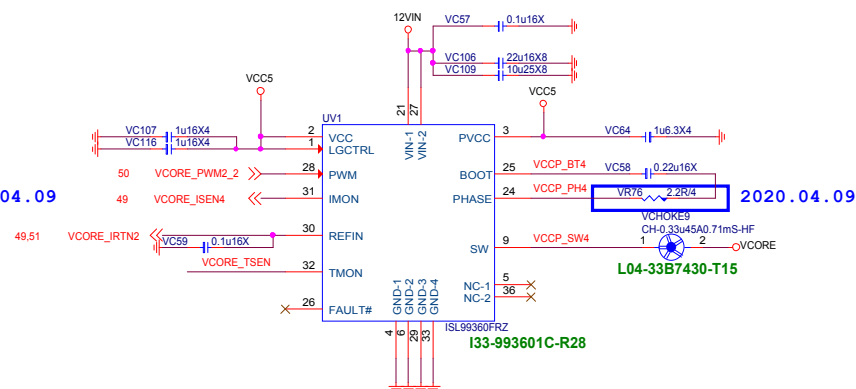
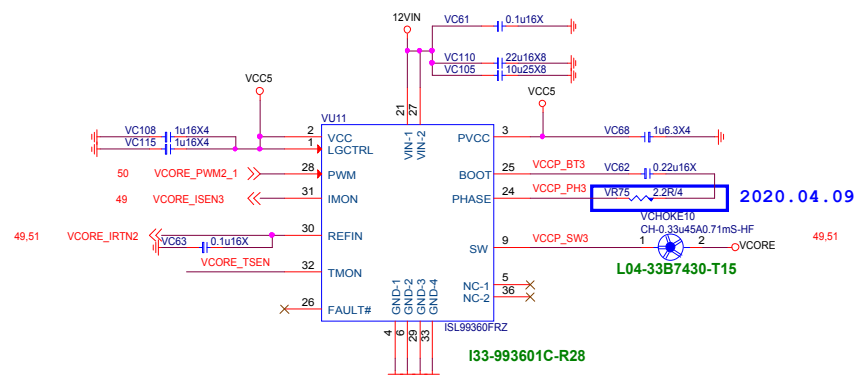


VCC Imax: 4.75mA  
IPVCC Imax: 15mA

Dr.MOS 3.3V Level



49.52 Vcore\_TSEN &lt;&lt; Vcore\_TSEN

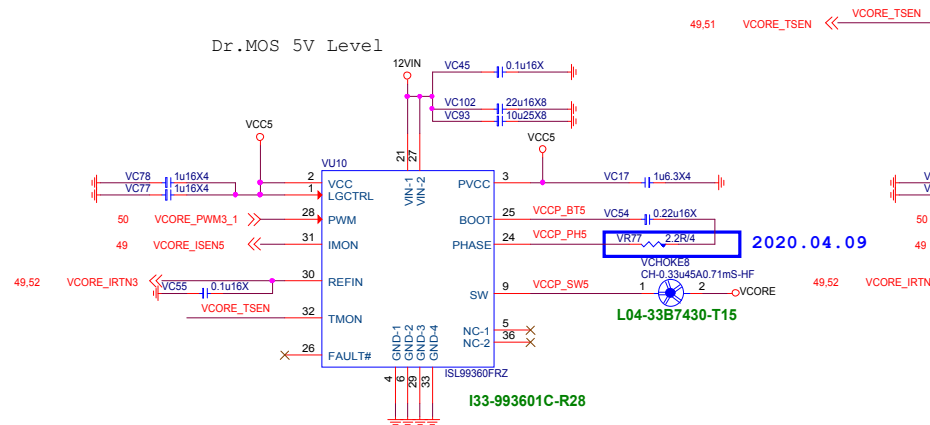


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Size	Document Description	Rev
Custom	CPU Power Vcore Phase 1-4	10
Date:	Tuesday, April 21, 2020	Sheet 51 of 78

Dr.MOS 5V Level



2020.04.09

L04-33B7430-T15

I33-993601C-R28

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L04-33B7430-T15

I33-993601C-R28

2020.04.09

L04-33B7430-T15

I33-993601C-R28

2020.04.09

L04-33B7430-T15

I33-993601C-R28

2020.04.09

L04-33B7430-T15

I33-993601C-R28

2020.04.09

L04-33B7430-T15

I33-993601C-R28

2020.04.09

L04-33B7430-T15

I33-993601C-R28

2020.04.09

L04-33B7430-T15

I33-993601C-R28

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L04-33B7430-T15

I33-993601C-R28

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L04-33B7430-T15

I33-993601C-R28

2020.04.09

L04-33B7430-T15

I33-993601C-R28

2020.04.09

L04-33B7430-T15

I33-993601C-R28

2020.04.09

L04-33B7430-T15

I33-993601C-R28

2020.04.09

L04-33B7430-T15

I33-993601C-R28

2020.04.09

L04-33B7430-T15

I33-993601C-R28

2020.04.09

L04-33B7430-T15

I33-993601C-R28

2020.04.09

L04-33B7430-T15

I33-993601C-R28

2020.04.09

L04-33B7430-T15

I33-993601C-R28

2020.04.09

L04-33B7430-T15

I33-993601C-R28

2020.04.09

L04-33B7430-T15

I33-993601C-R28

2020.04.09

L04-33B7430-T15

I33-993601C-R28

2020.04.09

L04-33B7430-T15

I33-993601C-R28

2020.04.09

L04-33B7430-T15

I33-993601C-R28

2020.04.09

L04-33B7430-T15

I33-993601C-R28

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L04-33B7430-T15

I33-993601C-R28

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L04-33B7430-T15

I33-993601C-R28

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L04-33B7430-T15

I33-993601C-R28

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L04-33B7430-T15

I33-993601C-R28

2020.04.09

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I33-993601C-R28

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L04-33B7430-T15

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L04-33B7430-T15

I33-993601C-R28

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L04-33B7430-T15

I33-993601C-R28

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L04-33B7430-T15

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L04-33B7430-T15

I33-993601C-R28

2020.04.09

L04-33B7430-T15

I33-993601C-R28

2020.04.09

L04-33B7430-T15

I33-993601C-R28

2020.04.09

L04-33B7430-T15

I33-993601C-R28

2020.04.09

L04-33B7430-T15

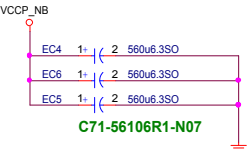
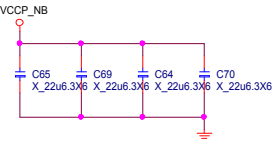
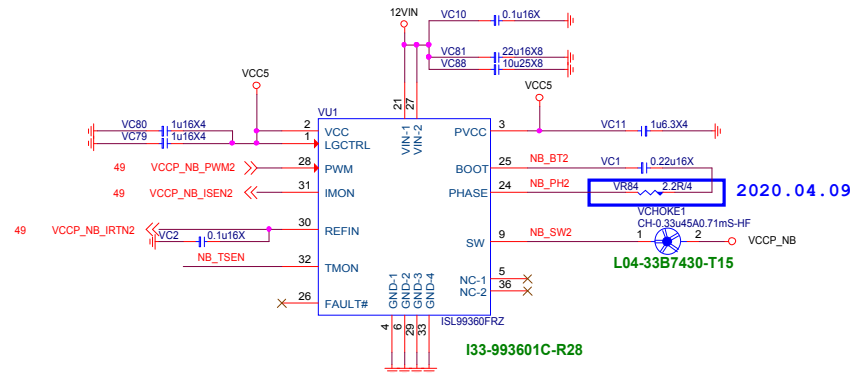
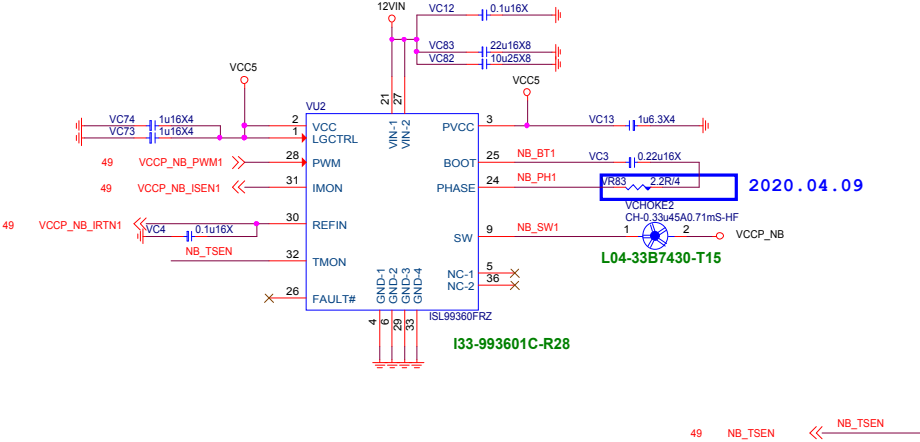
I33-993601C-R28

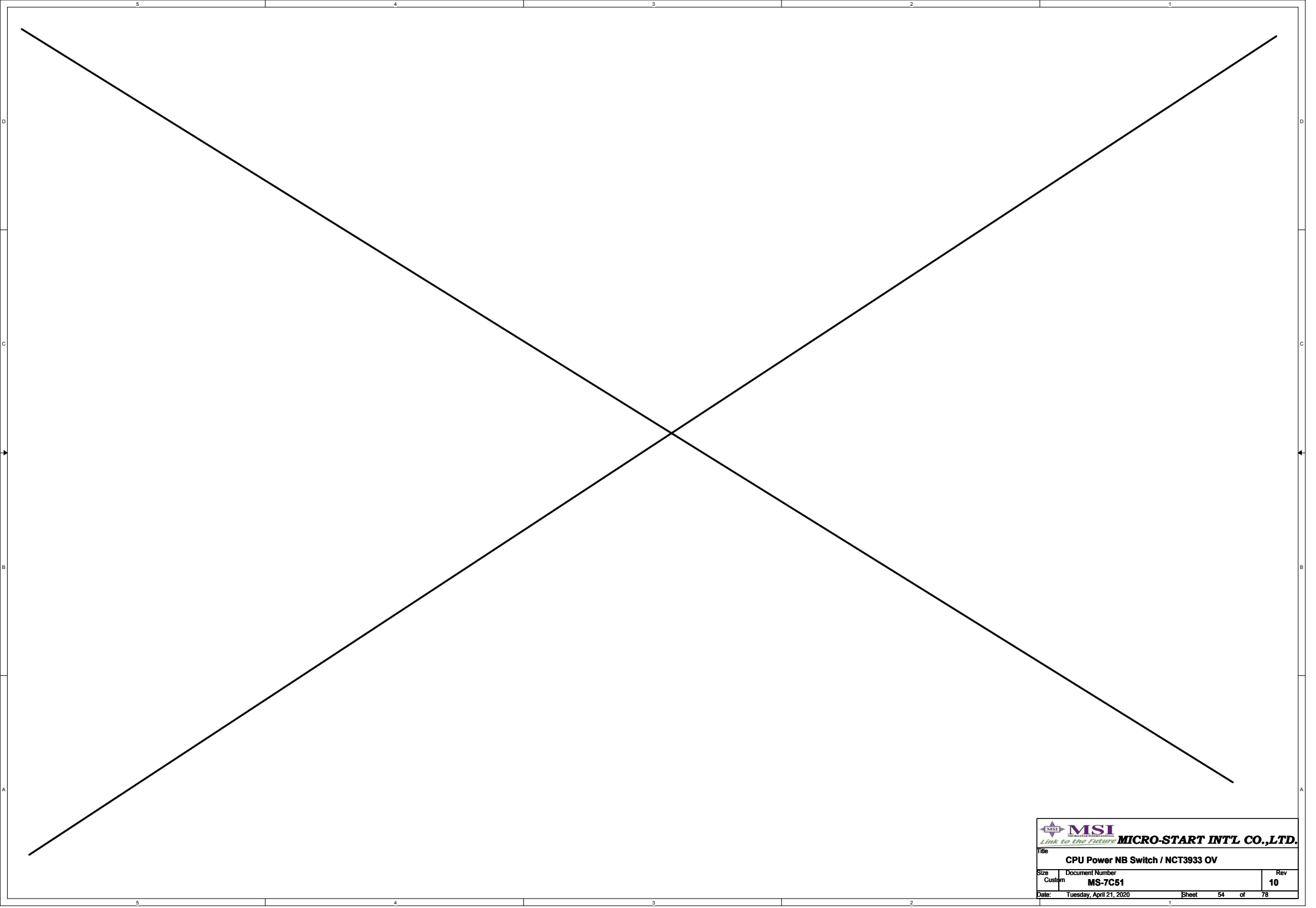
2020.04.09


L04-33B7430-T15

I33-993601C-R28

Dr.MOS 3.3V Level





 <b>MSI</b> <small>Micro-Start International Co., Ltd.</small>		
<i>Link to the Future</i> <b>MICRO-START INT'L CO.,LTD.</b>		
Title <b>CPU Power NB Switch / NCT3933 OV</b>		
Size	Document Number	Rev
Custom	<b>MS-7C51</b>	<b>10</b>
Date:	Tuesday, April 21, 2020	Sheet 54 of 78

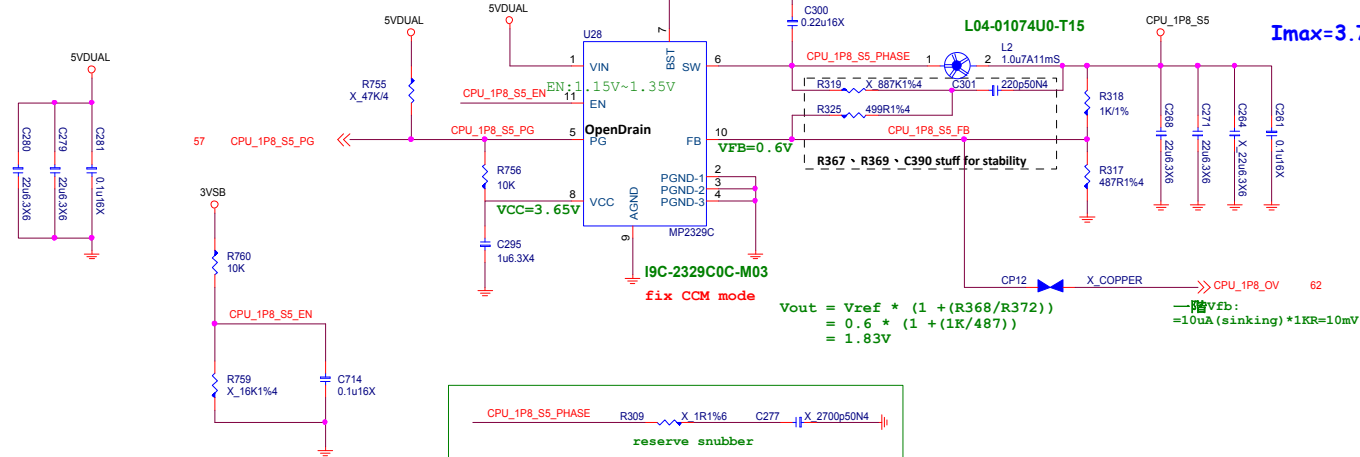
CPU 1.8V\_S5@0.5A  
CPU\_VDDP\_S5@1A  
AUDIO1.8V@0.25A

Input Current =  $(6.5A \cdot 1.8V) / 5V / 0.8 = 3A$

Continuous Conduction Mode (CCM)

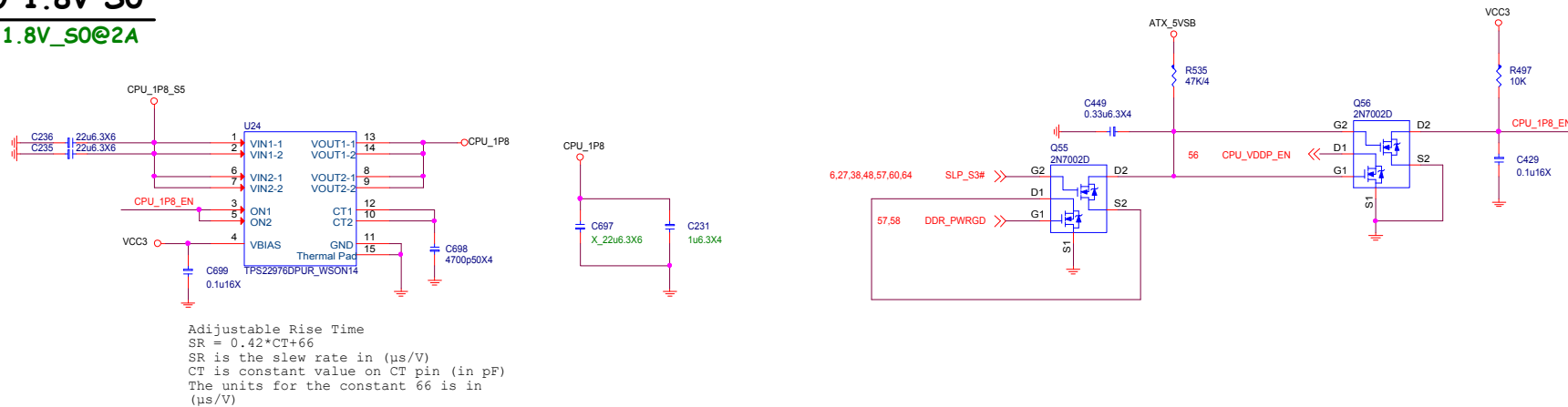
CPU\_1P8\_BST、CPU\_1P8\_BST\_R >50 mils.  
CPU\_1P8\_S5\_BST

**OCP = 6.5A**

$$I_{\max} = 3.75A(S_5 + S_0)$$


## CPU 1.8V S0

CPU 1.8V\_S0@2A



Adjustable Rise Time  
 $SR = 0.42 \cdot CT \cdot 66$   
 SR is the slew rate in ( $\mu\text{s}/\text{V}$ )  
 CT is constant value on CT pin (in pF)  
 The units for the constant 66 is in  
 ( $\mu\text{s}/\text{V}$ )



**MICRO-STAR INT'L CO.,LTD**

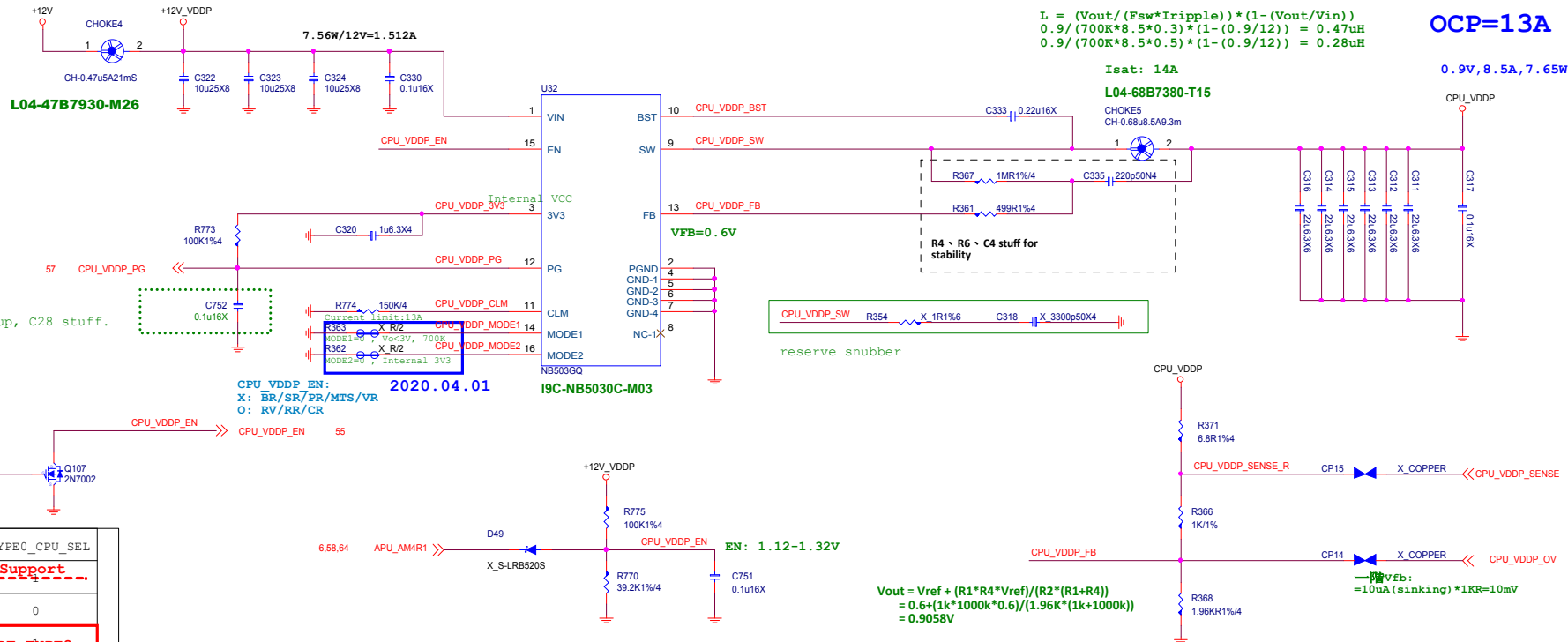
MS-7C91

Size Custom	Document Description <b>CPU Power 1.8_S0 / S5</b>	Rev 10
Date: Tuesday, April 21, 2020	Sheet 55 of 78	

# CPU\_VDDP\_S0

0.9V@S0:8.5A

Input Current = (13A\*0.9V)/12V/0.8 = 1.22A  
 Choke Isat = 8A  
 Irms=Iout\*SQRT((Vo/Vi)\*(1-(Vo/Vi)))  
 =13\*SQRT((0.9/12)\*(1-(0.9/12))) = 3.42A  
 Choke Irms = 5 A



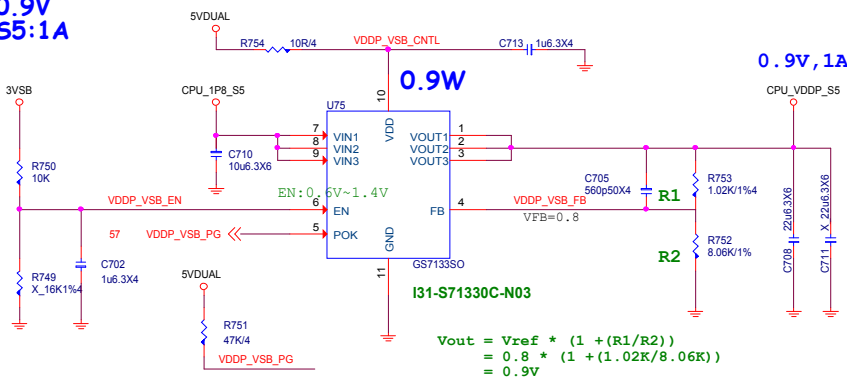
20180822  
 fix PG glitch when VCC3 ramp up, C28 stuff.

TYPE0\_CPU\_SEL  
 0: RV/RR/CR  
 1: BR/SR/PR/MTS/VR  
 TYPE1\_CPU\_SEL  
 1: TYPE 0  
 2: TYPE 2

CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	0
NA		0	0
SR	2	CPU VDDP1 NOT SUPPORT TYPE2	
RV/ZP	3	1	0
MTS	4	CPU VDDP1 NOT SUPPORT TYPE4	
RR	5	1	0
VM	6	CPU VDDP1 NOT SUPPORT TYPE6	
CR	7	1	0

# CPU\_VDDP\_S5

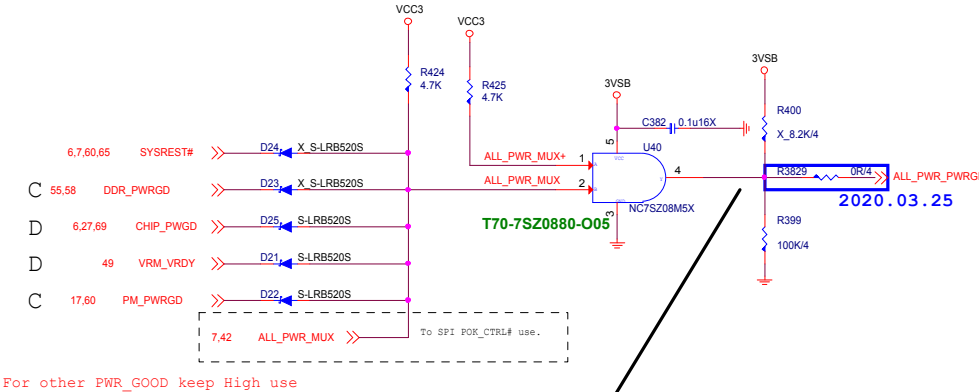
0.9V  
 S5:1A





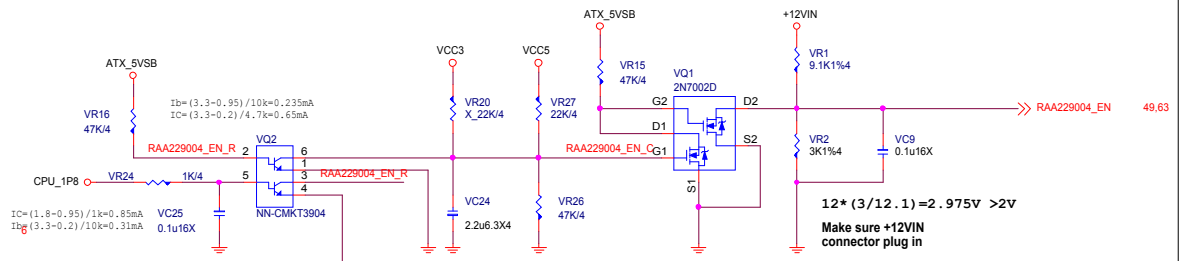
ALL POWER GOOD MUX

S0 PG



When you use external buffer then you cannot let APU PWR\_GOOD pin float in any sleep state. If you're buffer use 3.3V\_S0 and you need Pull-down 100K. If you're buffer use 3.3V\_S5 and you don't need PD.

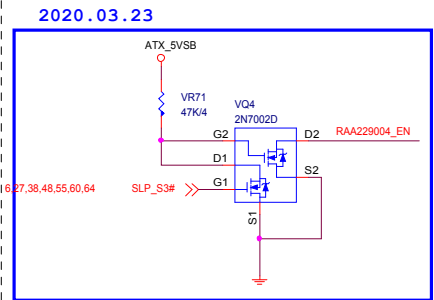
VRM\_Enable circuit



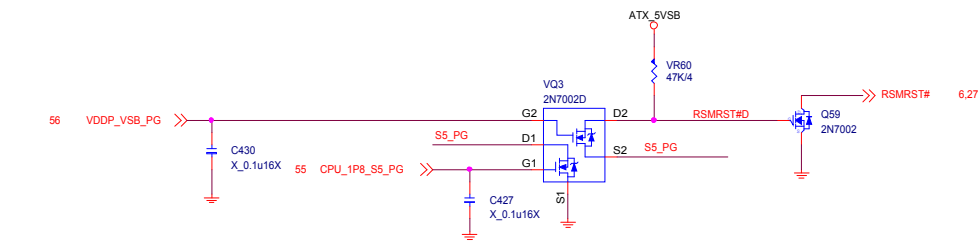
2020.03.23

6.7,56 TYPE\_CPU\_SEL

CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	0
NA	X	0	0
SR	2	CPU VDDP	NOT SUPPORT TYPE2
RV/ZP	3	1	0
MTS	4	CPU VDDP	NOT SUPPORT TYPE4
RR	5	1	0
VM	6	CPU VDDP	NOT SUPPORT TYPE6
CR	7	1	0



S5 PG



DDR4\_1.2V@28.7A

18A FOR CPU

9.5A FOR 4DIMM

1.2A FOR DDR VTT

Rocset=1.5\*Imax\*Rdson(Low side)/Iocset  
=1.5\*28.7A\*2mohm/10uA  
=8.61K

OCP = 43.05A; Choke Isat=43A

Rocset = 1.5 \* Imax \* Rdson(Low) / Iocset  
R639 = 1.5 \* 28.7 \* 2mohm / 10uA  
R639 = 8.61K

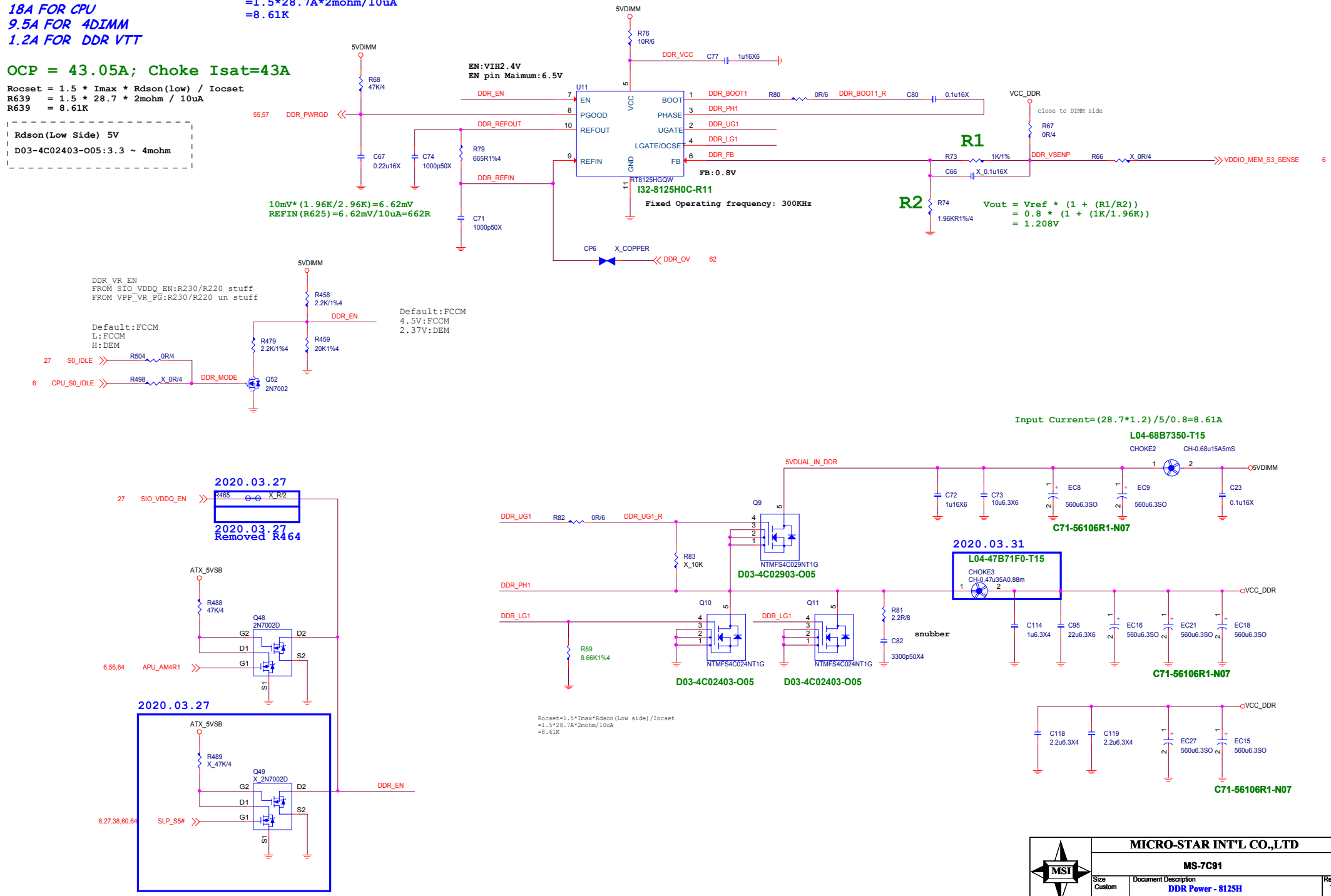
Rdson(Low Side) 5V  
D03-4C02403-005:3.3 ~ 4mohm

DDR VR\_EN  
FROM SIO\_VDDQ\_EN:R230/R220 stuff  
FROM VFP\_VR\_PG:R230/R220 un stuff

Default:FCCM  
L:FCCM  
H:DEM

Default:FCCM  
4.5V:FCCM  
2.37V:DEM

Rocset=1.5\*Imax\*Rdson(Low side)/Iocset  
=1.5\*28.7A\*2mohm/10uA  
=8.61K



Input Current=(28.7\*1.2)/5/0.8=8.61A

L04-68B7350-T15

CH0KE2 CH-0.68u15A5mS

C71-56106R1-N07

2020.03.31

L04-47B71F0-T15

CH0KE3 CH-0.47u35A0.88m

C71-56106R1-N07

C71-56106R1-N07

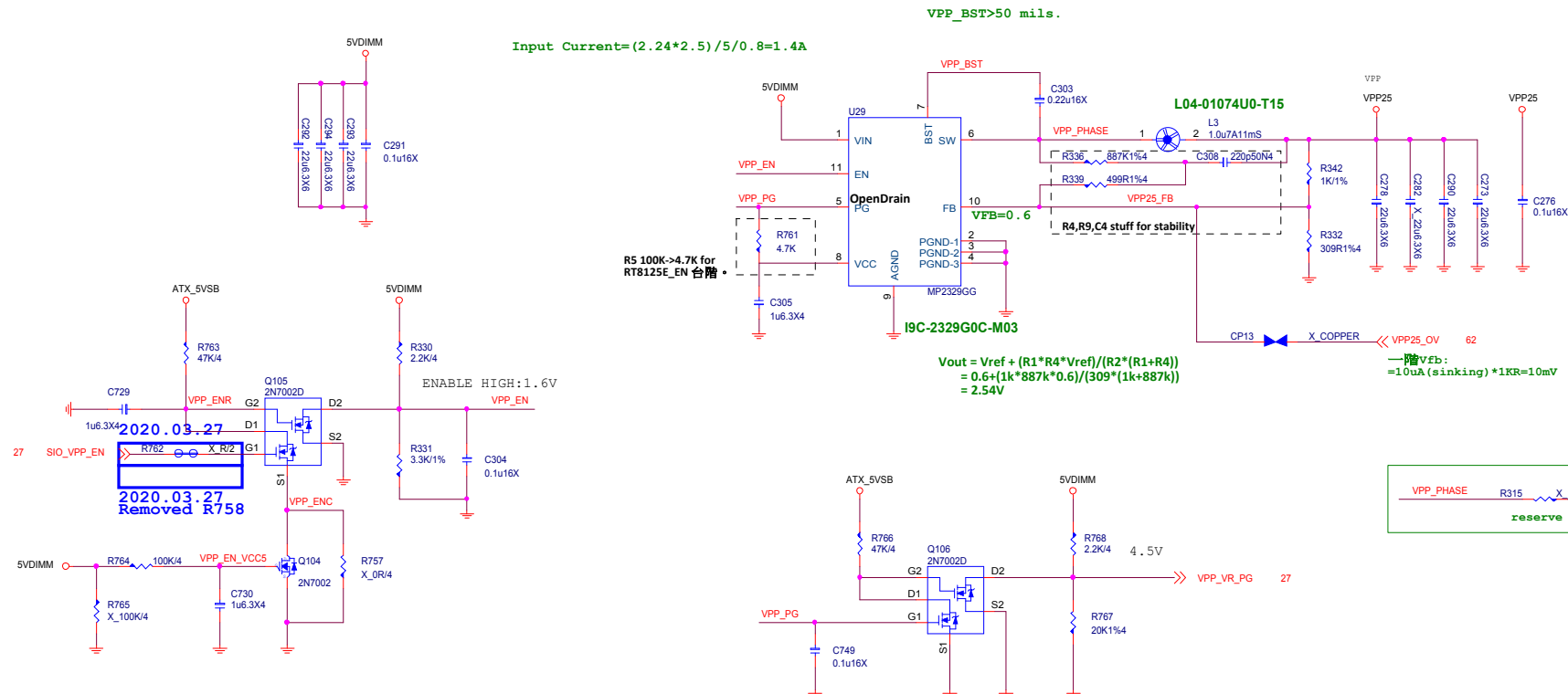


MICRO-STAR INT'L CO.,LTD

MS-7C91

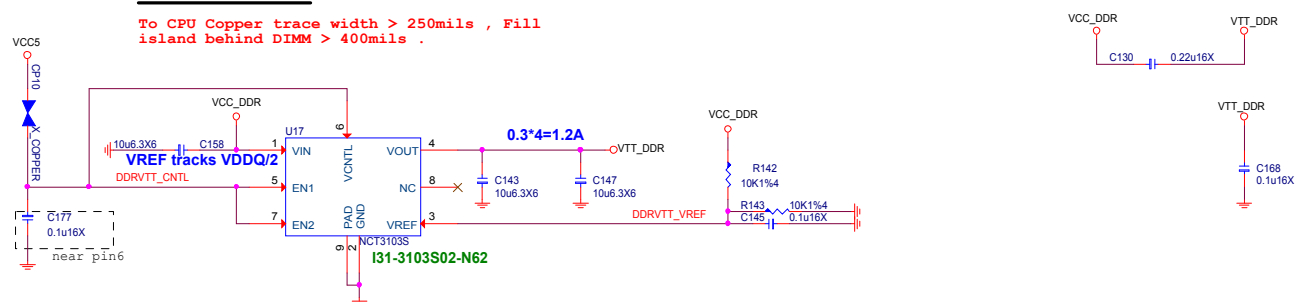
Size Custom Document Description DDR Power - 8125H Rev 10  
Date: Tuesday, April 21, 2020 Sheet 58 of 78

2.5V@2.24A



### DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



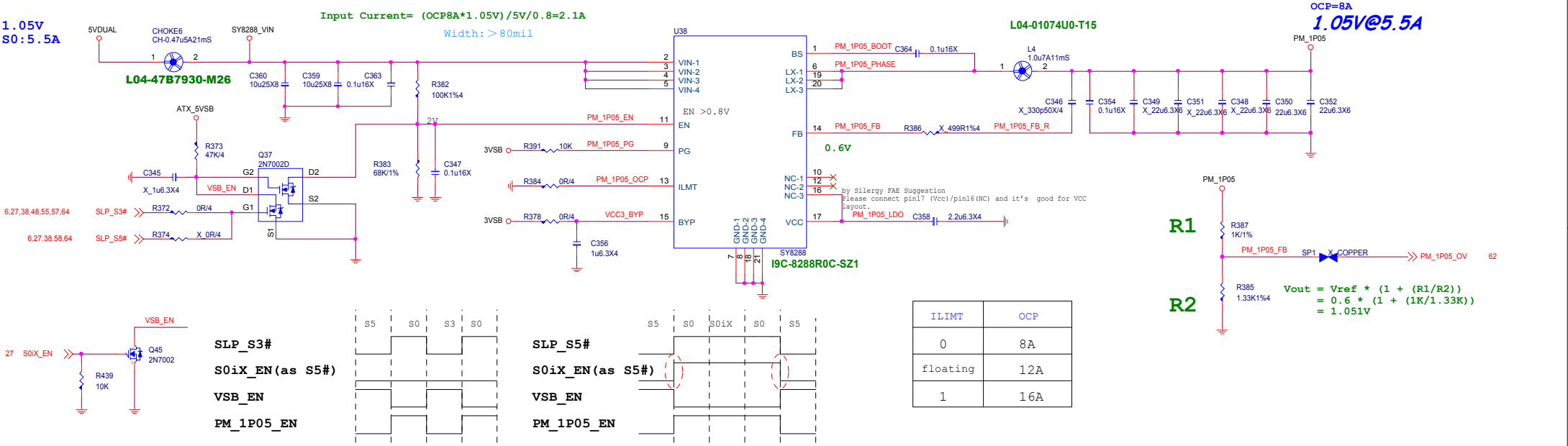
**MICRO-STAR INT'L CO.,LTD**

MS-7C91

Size Custom	Document Description <b>DDR VPP25 / VTT</b>	Rev 10
Date: Tuesday, April 21, 2020		Sheet 59 of 78

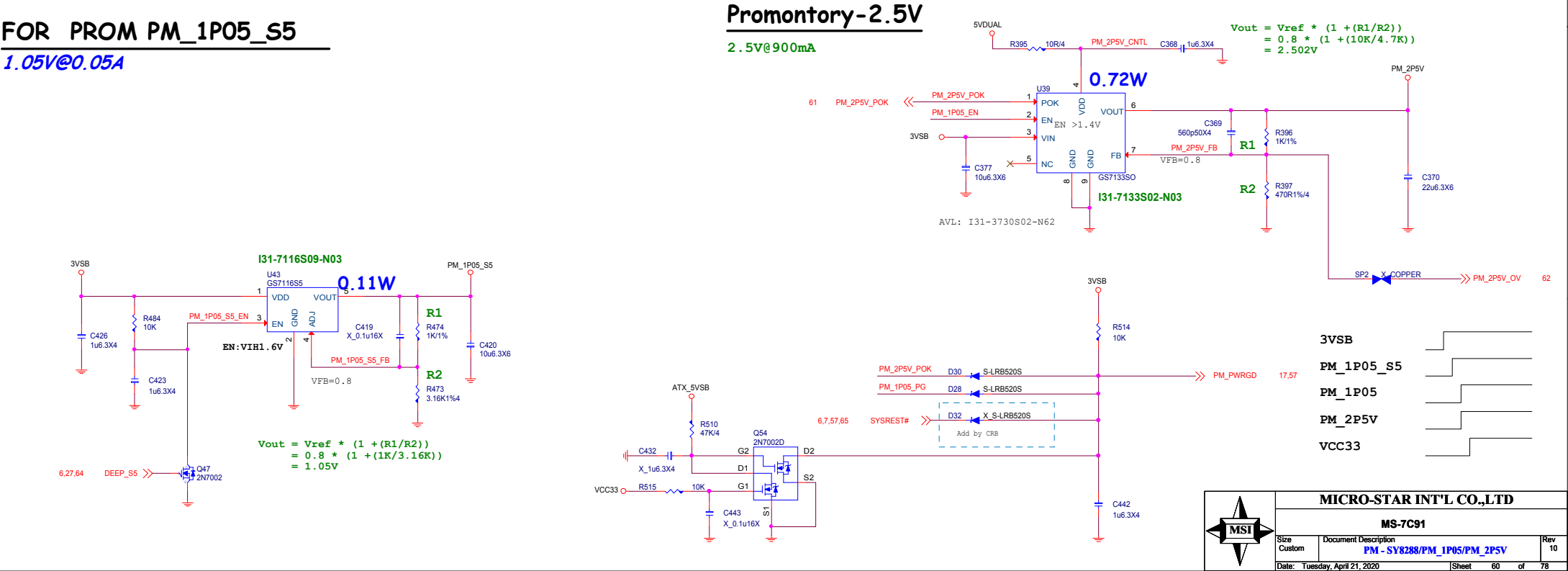
FOR Promontory 1.05V\_S0

1.05V  
S0:5.5A



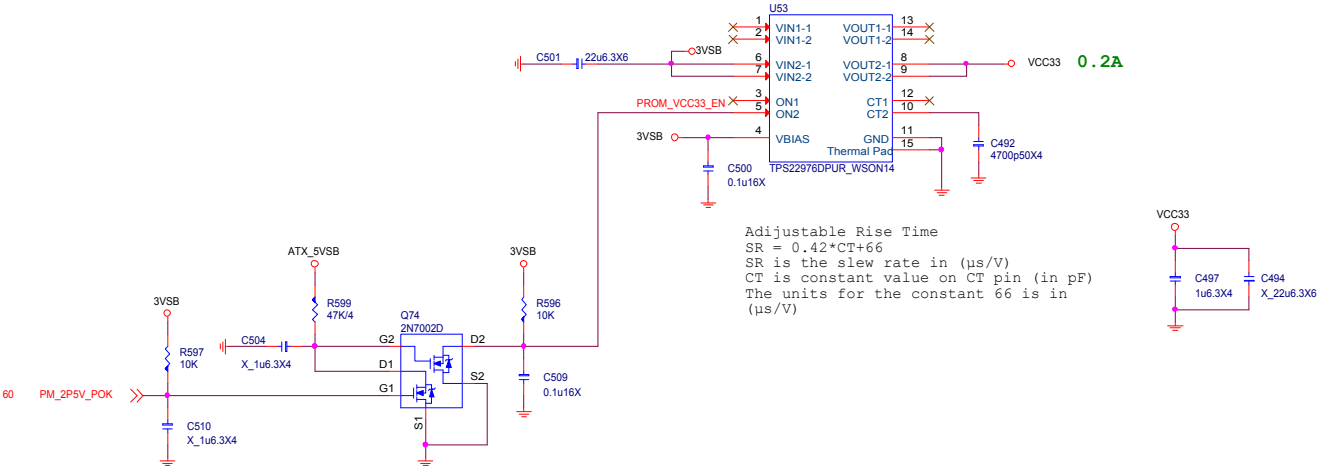
FOR PROM PM\_1P05\_S5

1.05V@0.05A



PROM VCC33

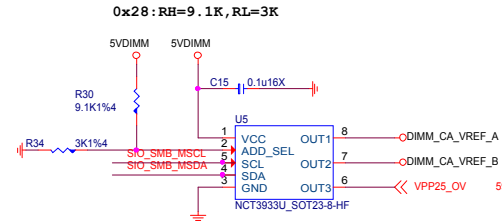
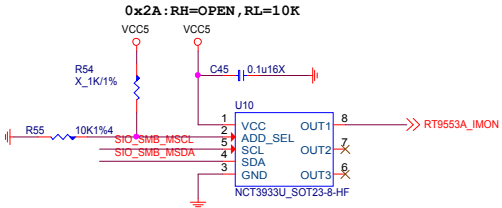
VCC33@0.2A



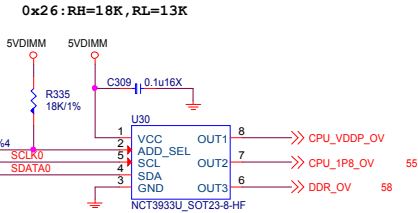
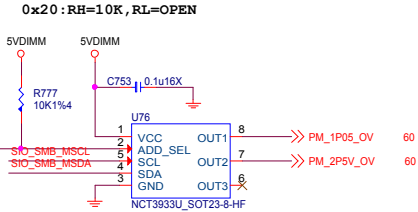
Over Voltage Control IC

UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

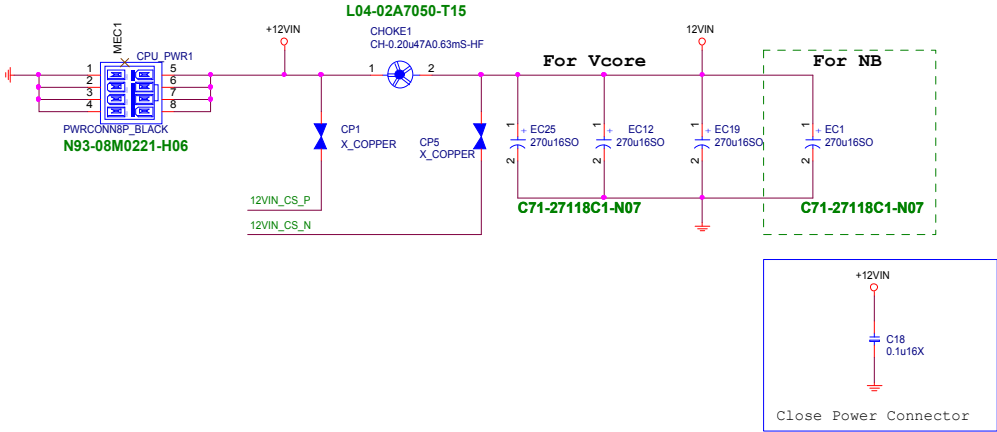


6.27.49 SIO\_SMB\_MSCLE SIO\_SMB\_MSCLE  
6.27.49 SIO\_SMB\_MSDA SIO\_SMB\_MSDA



6.11.24 SCLK0 SCLK0  
6.11.24 SDA0 SDA0

CPU POWER CONNECTOR



$$\Delta V_{ILIM} = 10\mu A * [ (60.4K * 40.2K) / (60.4K + 40.2K) ]$$
  
$$= 226mV$$

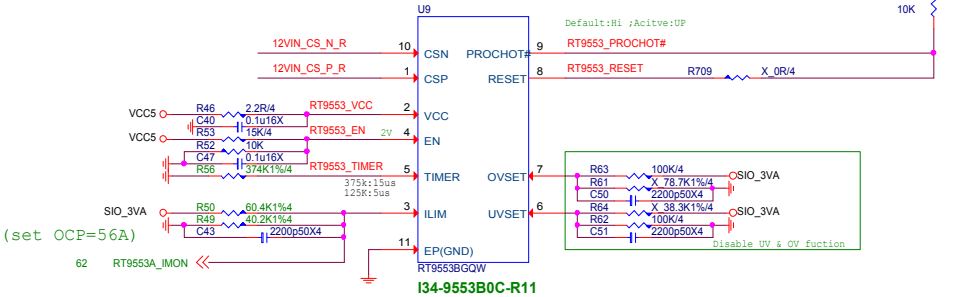
$$I_{sense} = V_{ILIM} / 100 * R_{sense}$$

$$\Delta I_{sense} = 226mV / 100 * 0.63m = 3.58A$$

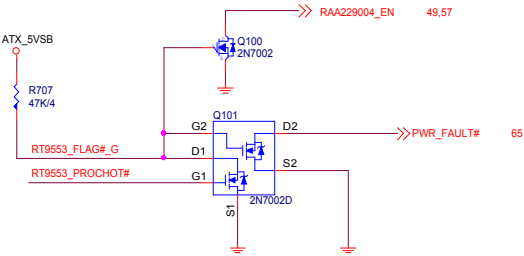
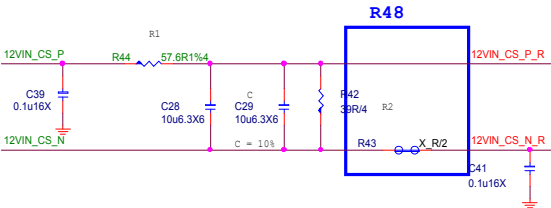
Vcore	SOC
$D = V_{out} / V_{in}$	$D = V_{out} / V_{in}$
$V_{in} = 12$ > input voltage	$V_{in} = 12$ > input voltage
$V_{out} = 2$ > output Vcore	$V_{out} = 1.55$ > output Vcore
$D = 0.166667$	$D = 0.129167$
$I_o = I_{core(max)} * 0.8$	$I_o = I_{core(max)} * 0.8$
$I_{core(max)} = 200$ > Vcore current	$I_{core(max)} = 75$ > Vcore current
$I_{avg} = 160$ A	$I_{avg} = 60$ A
$I_{ripple} = \{ I_o * \sqrt{D} * \sqrt{(1-D)} \} / \text{Phase}$	$I_{ripple} = \{ I_o * \sqrt{D} * \sqrt{(1-D)} \} / \text{Phase}$
Phase = 10 phase	Phase = 2 phase
$I_{ripple} = 5.962848$ A	$I_{ripple} = 10.06153$ A
How many pcs. Of Cap.	How many pcs. Of Cap.
$I_{ripple(cap)} = 4700$ m A	$I_{ripple(cap)} = 4700$ m A
$COE_{TEMP} = 1$	$COE_{TEMP} = 1$
Input Cap. = 2 pcs.	Input Cap. = 3 pcs.

RT9553B CURRENT SENSE

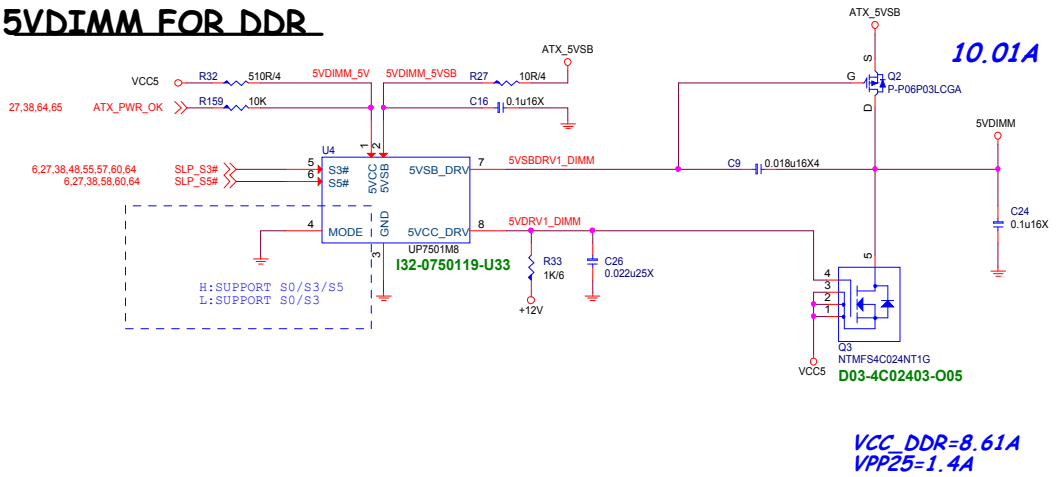
RT9553 PIN5: When start OV/UV, RESET delay time can meet SPEC 15us.



2020.03.25

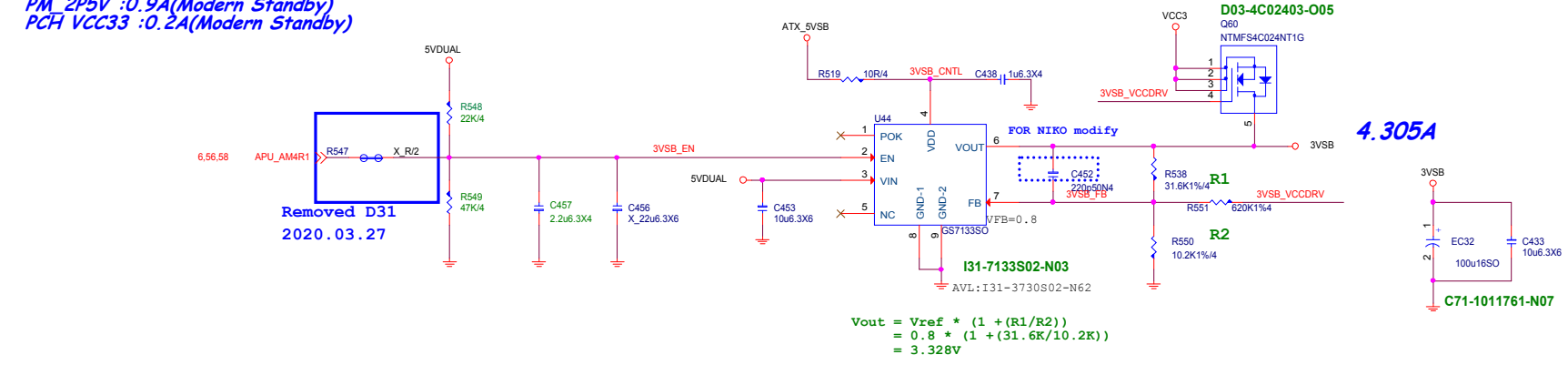


5VDIMM FOR DDR

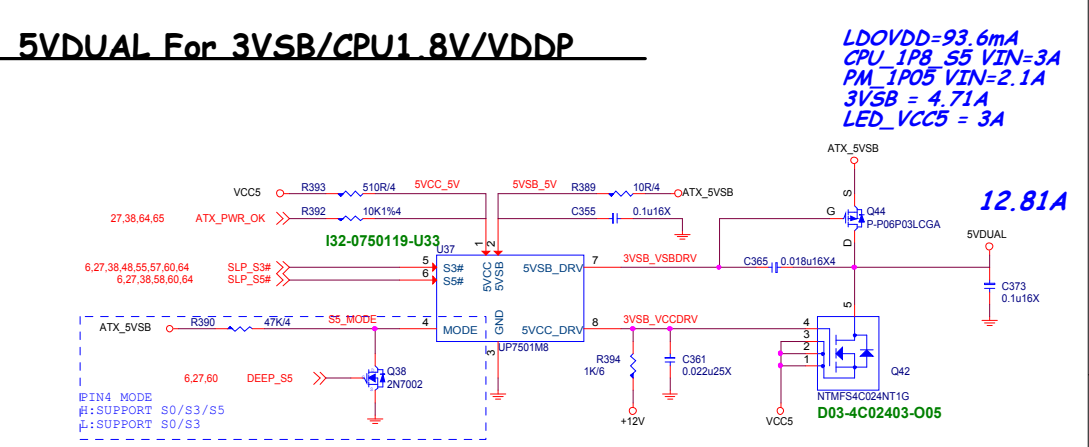


3VSB cost down  
3.3V@4.305A

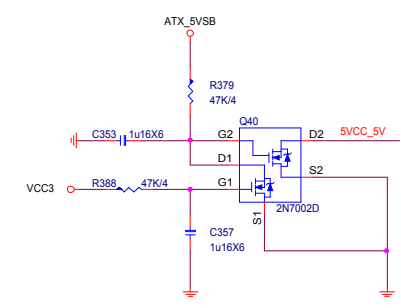
CPU:VDD\_33\_S5=0.25A  
CHIP:VDD\_33\_S5=0.07A  
PCIE=(375mA\*5)=1.875A  
M.2WIFI= 0.78A  
RT8111H LAN=0.18A  
PM\_1P05\_S5 :0.05A  
PM\_2P5V :0.9A(Modern Standby)  
PCH VCC33 :0.2A(Modern Standby)



5VDUAL For 3VSB/CPU1.8V/VDDP

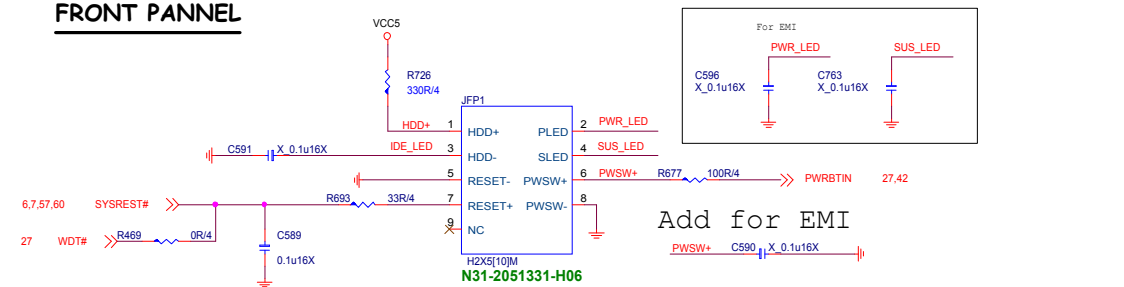


For power 700W solution (only for up7501+up7506 for 3VSB solution)  
The power supply VCC3 delay 12ms after VCC5 assert.  
The chip U7501 5VDRV1 work when the VCC5 ready  
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but  
VCC3 not ready and let the 3VSB sequence fail.





## FRONT PANNEL



ATX\_5VSB 5VDIMM

$I_b = (VCC3_{SB} - V_{be}) / (R535)$   
 $(3.3 - 0.95) / 1k = 2.35mA$   
 $I_c = (5VDIMM - V_{ce}) / R541$   
 $(5 - 0.2) / 330 = 14.5mA$

$S1b > I_c$

3VSB SIO\_3VA

R3798 X\_330R/6 R704 330R/6

R694 1K/4 R3800 X\_1K/4

SUS\_LED PWR\_LED

R695 4.7K R679 4.7K

Q97

2 SUSLED 3 PWRLED 4 5 LED\_VSB LED\_VCC

NN-CMKT3904

R3799 X\_330R/6 R698 330R/6

ATX\_5VSB 5VDIMM

$I_b = (VCC3_{SB} - V_{be}) / R529$   
 $(3.3 - 0.95) / 1k = 2.35mA$   
 $I_c = (5VDIMM - V_{ce}) / R530$   
 $(5 - 0.2) / 330 = 14.5mA$

$S1b > I_c$

3VSB SIO\_3VA

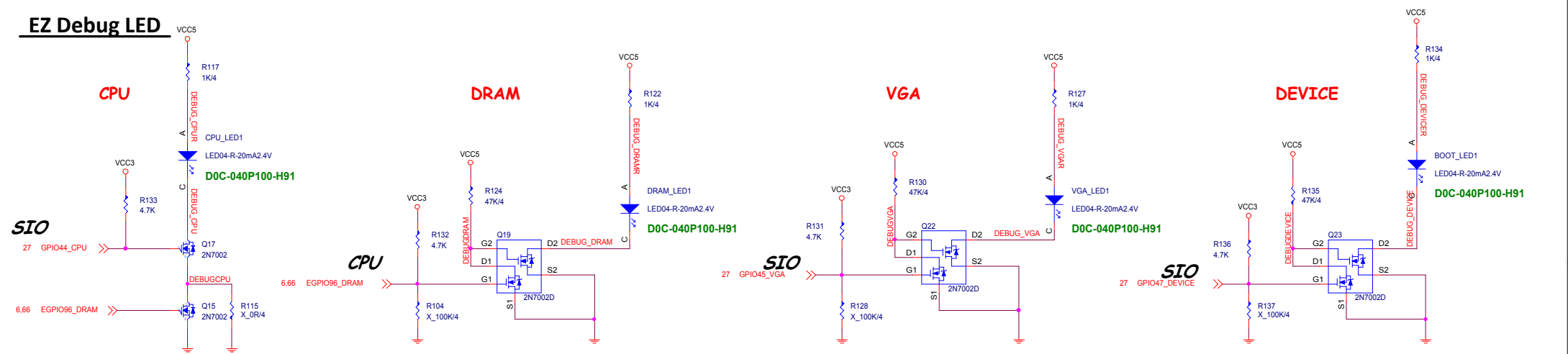
R680 1K/4 R3801 X\_1K/4

Reserve pull high to 5VDIMM if FM  
 don't want PWR\_LED light in deep mode

SIO ver. LAA  
 Push pull pin, no need



# EZ Debug LED



LED GPIO	GPIO44	EGPIO96	GPIO45	GPIO47	default Input
亮	OPEN-Drain	GPO LOW	GPO LOW	GPO LOW	
滅	GPO LOW	GPO HIGH	OPEN-Drain	OPEN-Drain	

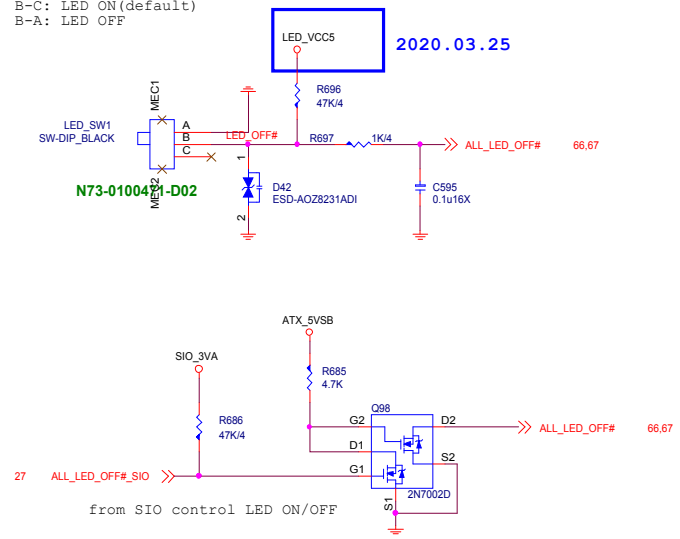
LED亮燈時同時將CPU LED關掉

## LED\_SW1 FORM SIO

D0C-040P100-H91/D0C-040S500-E07

### LED\_SW1 for ALL LED OFF

B-C: LED ON(default)  
B-A: LED OFF



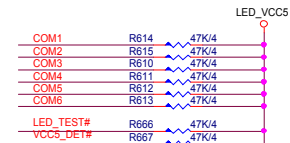
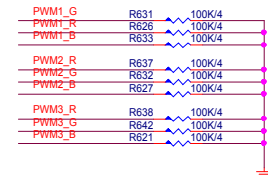
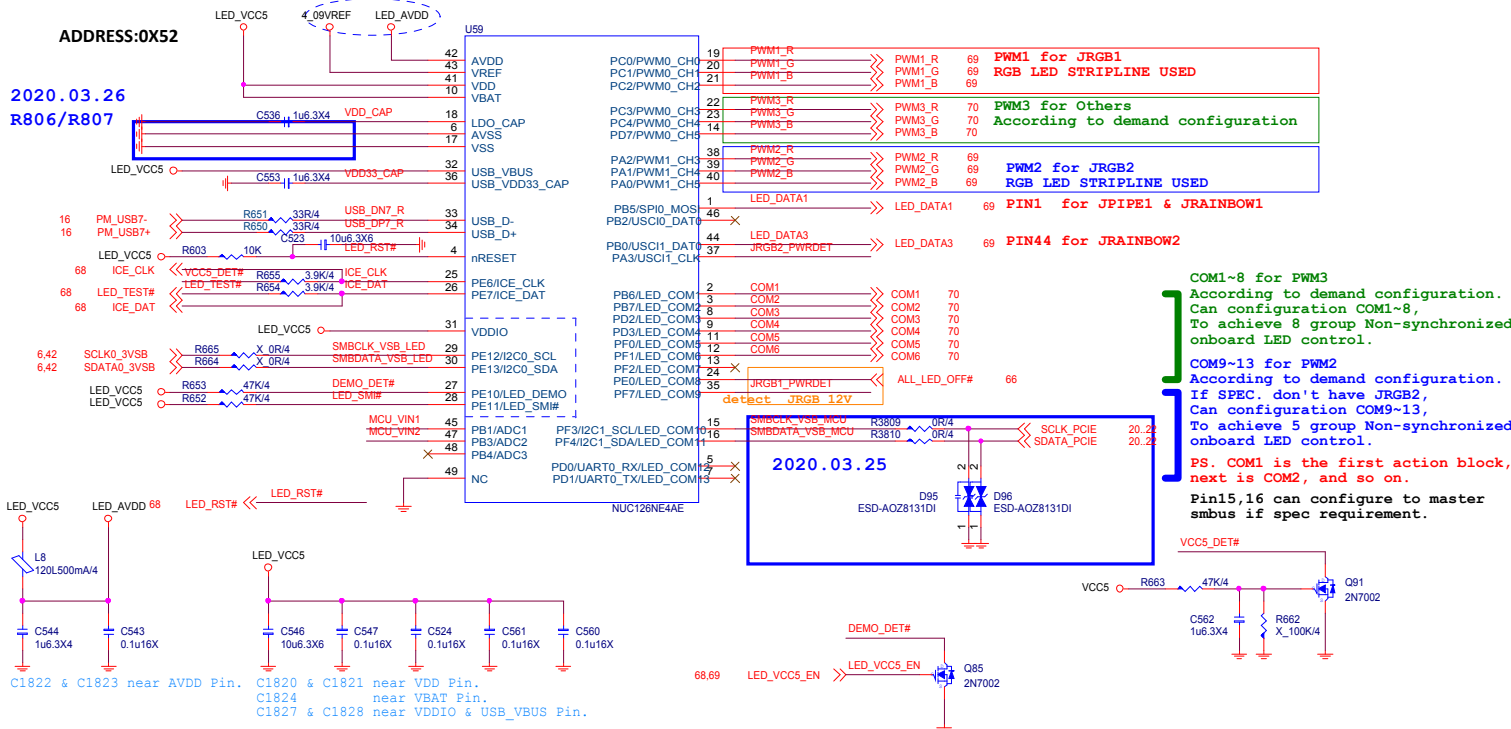
## 48 PIN LED MCU

If you use ADC function, need to separate VREF from AVDD and 4 09VREF stuff for VREF.

**ADDRESS:0X52**

2020.03.26

R806/R807

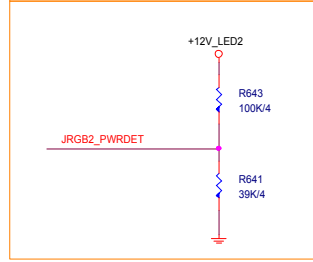
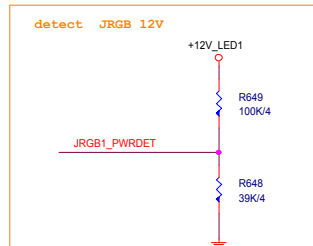


COM1-8 for PWM3  
According to demand configuration.  
Can configuration COM1-8,  
To achieve 8 group Non-synchronized  
onboard LED control.

COM9-13 for PWM2  
According to demand configuration.  
If SPEC. don't have URGEB,  
Can configuration COM9-13,  
To achieve 5 group Non-synchronized  
onboard LED control.

PS. COM1 is the first action block,  
next is COM2, and so on.

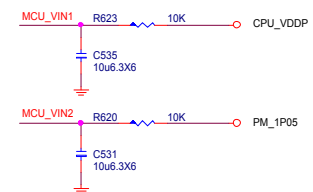
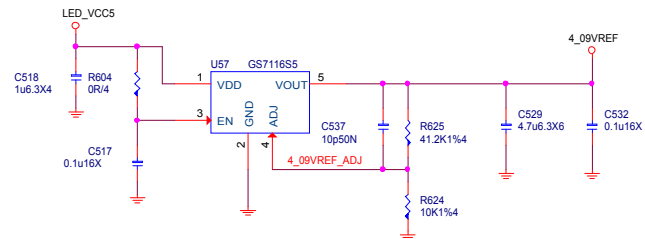
Pin15,16 can configure to master  
smbus if spec requirement.



## Clear MCU Circuit



Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~13	PWM2

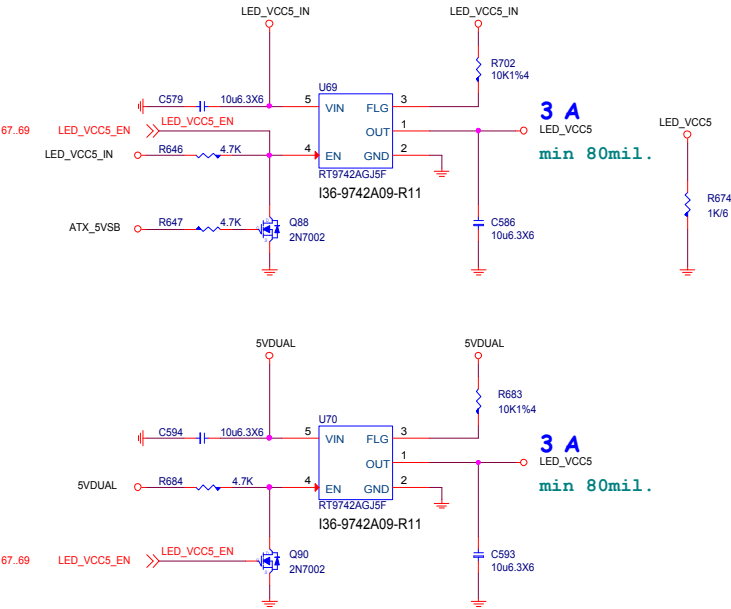


**MICRO-STAR INT'L CO.,LTD**

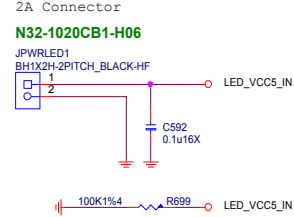
MS-7C91

Size Custom	Document Description <b>MCU - LED Control</b>	Rev 10
Date: Tuesday, April 21, 2020		Sheet 67 of 78

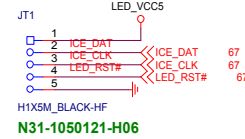
EXTERNAL POWER INPUT



External Power



JT1 for FW update



JF1 for Factory test



[illegible][illegible]

The image shows a PCB layout for the JRAINBOW1 module, featuring two identical LED driver circuits. The layout is based on a 60mil grid.

**Top Circuit (U61):**

- IC:** RT9742AGJ5F (U61)
- Inputs:** VIN (5V), EN (VCC5\_LED\_EN3)
- Outputs:** OUT (3A), FLG (VCC5\_LED3)
- Components:** C551 (10u6.3X8), R629 (4.7K), C549 (X\_0.1u16X), R628 (10K1%4), C558 (10u6.3X6)
- LED:** Q79 (2N7002)

**Bottom Circuit (U62):**

- IC:** RT9742AGJ5F (U62)
- Inputs:** VIN (LED\_VCC5\_IN), EN (LED\_VCC5\_EN)
- Outputs:** OUT (3A), FLG (VCC5\_LED3)
- Components:** C550 (10u6.3X6), R630 (10K1%4), C557 (10u6.3X6)
- LED:** Q80 (2N7002)

**LED Driver Details:**

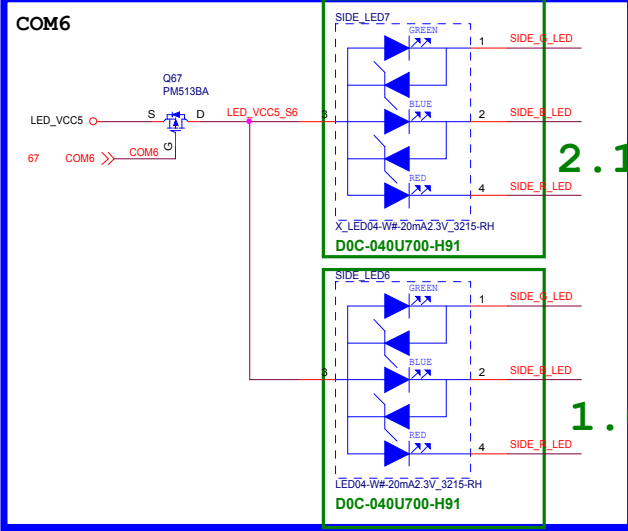
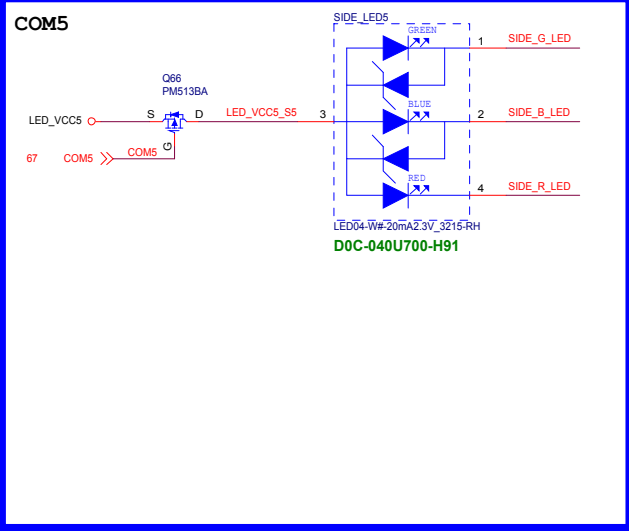
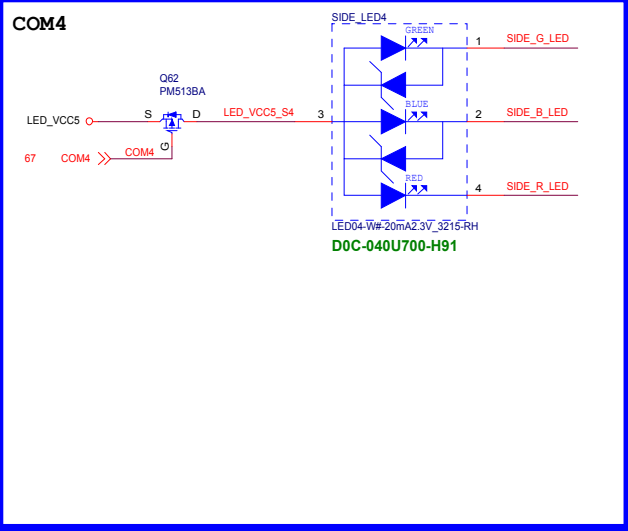
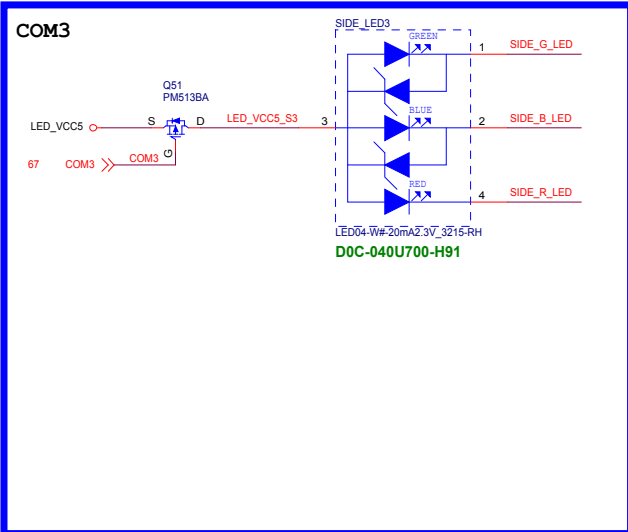
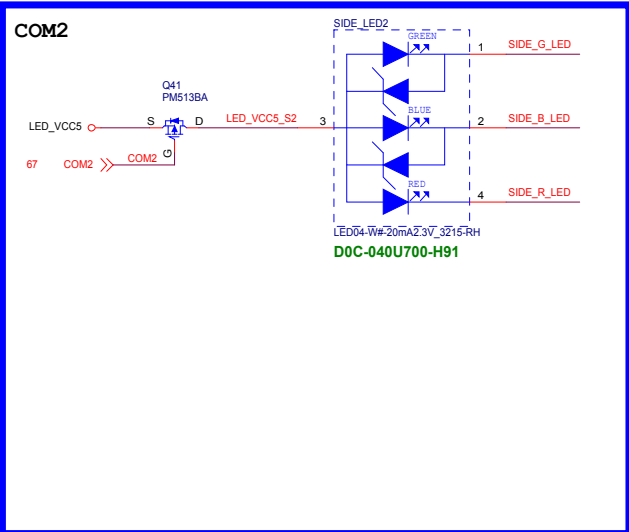
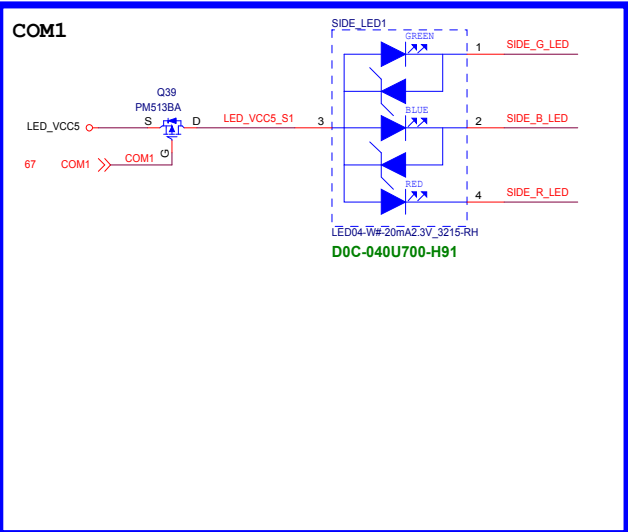
- LED:** H1X4[3]M\_BLACK-RH-1 (N31-1041111-P05)
- Current:** 3A
- Resistor:** R630 (10K1%4)
- Capacitor:** C557 (10u6.3X6)

**Other Components:**

- Resistor:** R629 (4.7K)
- Capacitor:** C549 (X\_0.1u16X)
- Resistor:** R628 (10K1%4)
- Capacitor:** C558 (10u6.3X6)
- Capacitor:** C550 (10u6.3X6)
- Capacitor:** C551 (10u6.3X8)
- Capacitor:** C557 (10u6.3X6)
- Capacitor:** C558 (10u6.3X6)
- Capacitor:** C559 (10u6.3X6)
- Capacitor:** C560 (10u6.3X6)
- Capacitor:** C561 (10u6.3X6)
- Capacitor:** C562 (10u6.3X6)
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- Capacitor:** C566 (10u6.3X6)
- Capacitor:** C567 (10u6.3X6)
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- Capacitor:** C569 (10u6.3X6)
- Capacitor:** C570 (10u6.3X6)
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- Capacitor:** C579 (10u6.3X6)
- Capacitor:** C580 (10u6.3X6)
- Capacitor:** C581 (10u6.3X6)
- Capacitor:** C582 (10u6.3X6)
- Capacitor:** C583 (10u6.3X6)
- Capacitor:** C584 (10u6.3X6)
- Capacitor:** C585 (10u6.3X6)
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- Capacitor:** C617 (10u6.3X6)
- Capacitor:** C618 (10u6.3X6)
- Capacitor:** C619 (10u6.3X6)
- Capacitor:** C620 (10u6.3X6)
- Capacitor:** C621 (10u6.3X6)
- Capacitor:** C622 (10u6.3X6)
- Capacitor:** C623 (10u6.3X6)
- Capacitor:** C624 (10u6.3X6)
- Capacitor:** C625 (10u6.3X6)
- Capacitor:** C626 (10u6.3X6)
- Capacitor:** C627 (10u6.3X6)
- Capacitor:** C628 (10u6.3X6)
- Capacitor:** C629 (10u6.3X6)
- Capacitor:** C630 (10u6.3X6)
- Capacitor:** C631 (10u6.3X6)
- Capacitor:** C632 (10u6.3X6)
- Capacitor:** C633 (10u6.3X6)
- Capacitor:** C634 (10u6.3X6)
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- Capacitor:** C664 (10u6.3X6)
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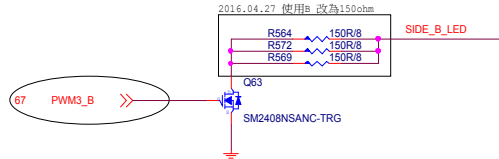
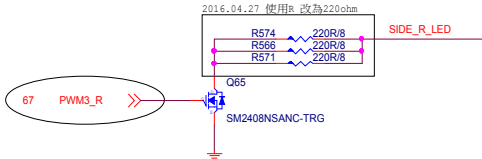
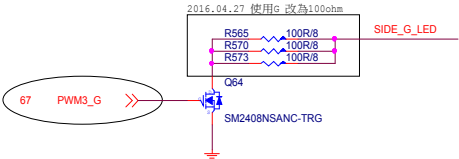
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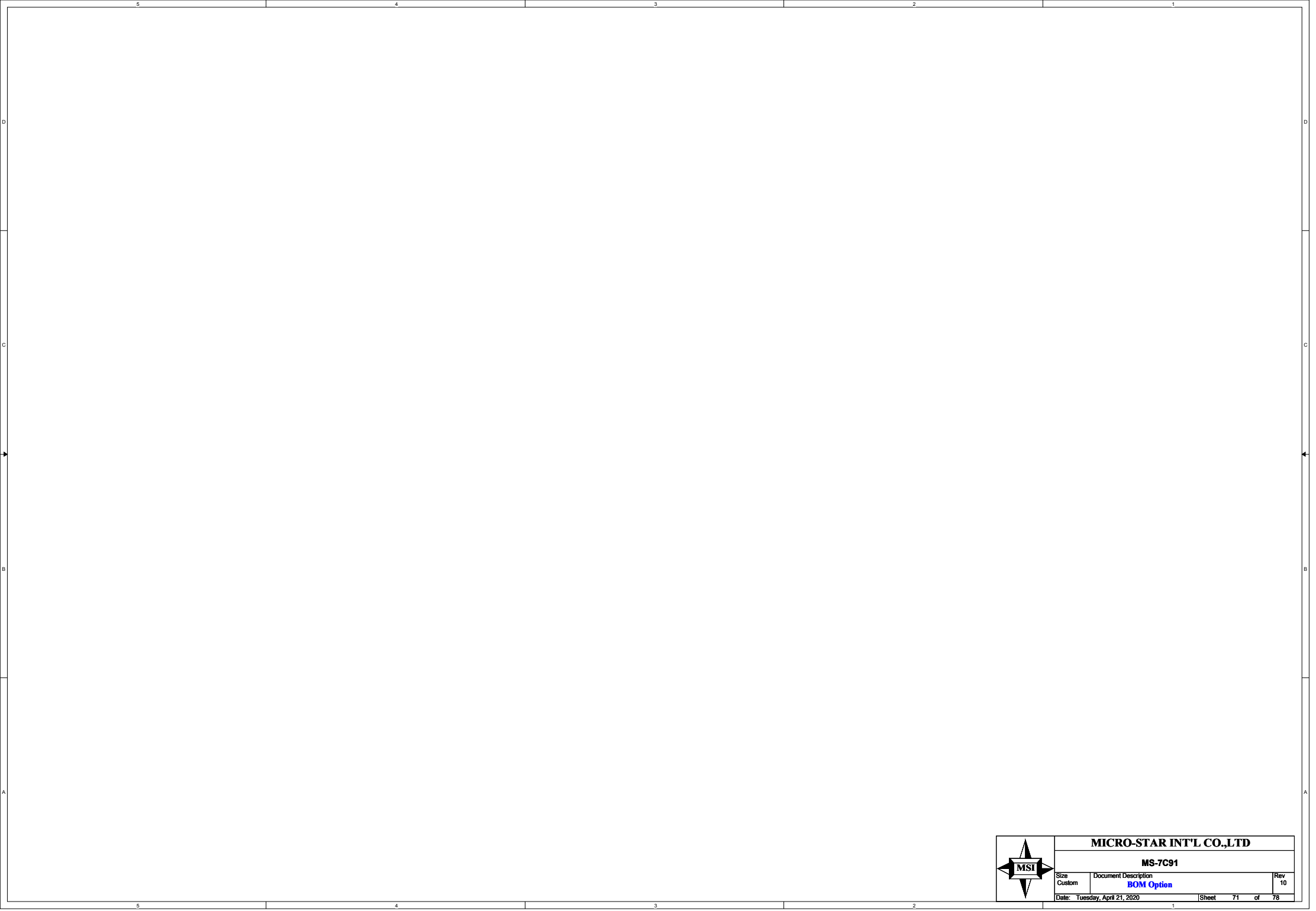
BOARD SIDE LED \*6




2.1 BOM

1.0 BOM





			<b>MICRO-STAR INT'L CO.,LTD</b>		
			<b>MS-7C91</b>		
Size	Document Description				Rev
Custom	<b>BOM Option</b>				10
Date: Tuesday, April 21, 2020			Sheet	71	of 78

CPU Socket



E95-0000022-A91

PCB

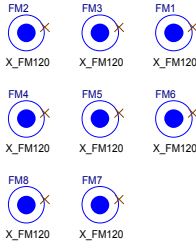
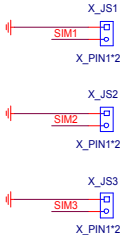
PCB



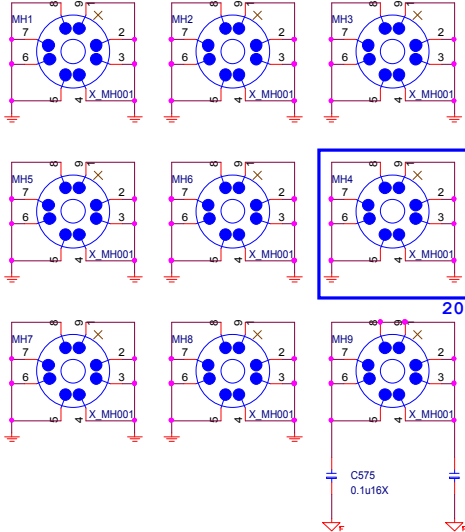
7C91\_21

PD0-07C9121-E48  
PD0-07C9121-G37

Simulation



Optics Orientation Holes



2020.04.15

MANUAL PART

AMI\_LAB1  
G51-M1SPXXA-A09  
G51-M1SPXXA-A09

CFOS1  
Y02-MU00170-CFO  
Y02-MU00170-CFO

HDMI\_LA1  
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HDMI  
HDMI LABEL  
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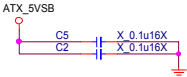
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Label  
MKT LABEL  
X\_MKT LABEL  
G51-M1SPP78-Q13



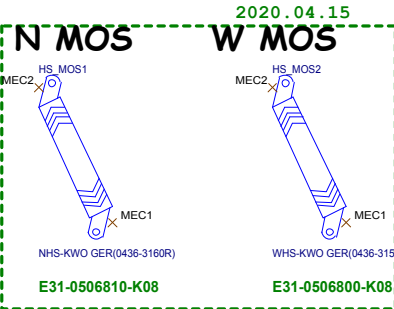
AVL:  
D06-0100161-F52  
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Moat CAP

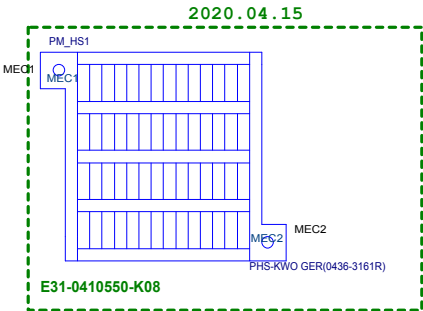
Reserve for bypass 12VIN noise use



MOS HEATSINK



PCH HEATSINK



M2 COVER

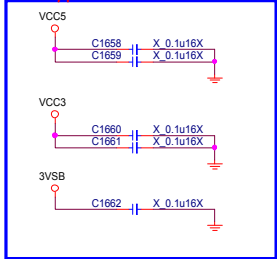
IO BRACKET

DDR COVER



20190201 Remove DDR\_COVER1

Reserve for bypass VCC5/VCC3/3VSB noise use



2020.04.14